Tailoring Strain in Microelectronic Devices

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ABSTRACT

The central device of this thesis is the transistor. It acts like a faucet, but then for electric charge. There is a connection that is called the source, just like the water company. And the charge flows into the drain. Finally there is a handle, here called the gate, to control the flow of charge.

The transistor is not an ideal faucet for electrons. For example, even when the gate is closed a very small current of electric charge flows through the device. This is the leakage current. In many modern electronics integrated circuits are used which may contain more than a billion of these transistors. Even if only a small leakage current flows through each of these transistors this may sum up to an altogether large leakage current. This leakage current is responsible for the static, or standby, power consumption of integrated circuits. Nowadays this static power is becoming one of the major energy consumers in integrated circuits.

One way to reduce the static power consumption the use of transistors that have an equal maximum flow of current, however, a smaller leakage current. This is the aim of the so-called small subthreshold swing transistors.

Many different small subthreshold swing concepts exist. They can be differentiated by either the way the charge is transported through the device, or the way in which the gate controls the potential of the channel. In this thesis we contribute to the latter group by proposing an innovative concept in which the control of the gate over the channel is amplified with mechanical strain. When compared to the faucet it is like the addition of a mechanical gearbox between the control knob and the actual piston blocking the water.

To understand the concept we have to explain the fin shaped field effect transistor (FinFET) first. This device has been recently introduced into mass production. It is as a fin shaped conventional field effect transistor (FET). The gate surrounds the complete fin and thus has an excellent control over the charge in the channel. As a result the FinFET is able to achieve a subthreshold swing of 60 mV/dec at room temperature, which is the limit for conventional transistors.

In these fin shaped field effect transistors mechanical strain is permanently present which enhances the carrier mobility. We studied a typical fin shaped field effect transistor from NXP-TSMC Research. During the front-end-of-line integration of these transistors a thin layer of titanium-

nitride (TiN) is deposited as a gate at an elevated temperature. When cooled down this material shrinks faster than the silicon. This compresses the silicon fin, resulting into negative strain. These devices have been made with various fin widths. Devices with a smaller fin width have a smaller volume of silicon compared to the volume of the TiN gate. Therefore, a device with a small fin width receives a larger amount of strain.

This strain moves down the silicon conduction band edge. This is counteracted by a secondary effect, quantum confinement. Due to the laws of quantum mechanics the electron in a narrow FinFET has to reside at an a certain energy above the band edge. This appears as a higher effective conduction band. Both the quantum confinement and strain effect on the leakage current are confirmed by measurements of the conduction band offset in narrow fins.

In a piezoelectric material an internal strain, or stress, builds up as function of the electric field. We propose to clamp the FinFET between two piezoelectric layers, and bias the piezoelectric layer with the gate source voltage of this FinFET. The piezoelectric layers expand, resulting in a compression of the fin with increasing V_{GS}. We call this effect strain modulation. The strain modulation moves down the conduction band edge as the device is turned on. We employ both an analytical model, and simulations (TCAD, FEM) to show that the strain modulated FinFET is capable to move the thermal limit of the subthreshold swing to 50 mV/dec at room temperature. Hence the proposed strain modulated FinFET adds an alternative path for small subthreshold swing devices.

In the thesis we also verify that the parameters which are used to describe the equations of motion in a piezoelectric resonator also hold for the static displacement. Furthermore we present and apply a method to extract the second order parameters from the resonance measurements under various bias conditions.

The choice of materials and structures for the strain modulated FinFET is not a straightforward task. A piezoelectric layer is required that is able to exert a large force, and a semiconductor that shows a large band deformation per applied force. Furthermore the two materials should be combined in such a way that the applied force effiently displaces the conduction band edge.

Finally, the effectiveness of strain modulation as a concept is evaluated. Inducing strain requires energy. As the strain is proportional to the applied gate source voltage each time the transistor switches state, energy is lost to straining the transistor. Therefore strain modulation increases the dynamic power, however, reduces the static power due to the lower leakage current.

SAMENVATTING

Dit proefschrift behandelt de transistor. Dit elektronisch apparaatje kun je vergelijken met een waterkraan, maar dan voor elektrische lading. Er is een aanvoer (genaamd source), een afvoer (drain), en een knop om de stroom door het kanaal van de transistor te kunnen regelen, deze noemen we de gate.

Deze elektrische kraan is niet ideaal. Dit blijkt onder andere wanneer je probeert deze kraan helemaal dicht te draaien. Hoe hard je hem ook dicht schroeft, er zal altijd een kleine lekstroom door de transistor heen blijven lopen.

Ondanks dat deze zeer klein is, is de lekstroom wel erg belangrijk. Een modern geïntegreerd circuit (zoals bijvoorbeeld een computerchip) bevat enkele miljarden transistoren. Tel de lekstroom van al die transistoren bij elkaar op en je kunt je voorstellen dat de totale lekstroom fors is. De totale lekstroom is evenredig met het statisch vermogen, welke tegenwoordig een groot deel van het totale energieverbruik van geïntegreerde circuits voor zijn rekening neemt.

Een manier om dit statische vermogen te verminderen is het gebruik van zogenaamde kleine subthreshold swing transistoren. Het idee is dat ze net zo goed stroom kunnen geleiden, maar dat ze minder lekstroom hebben. Er zijn vele voorbeelden van dit soort transistoren. Sommigen gebruiken een andere manier van ladingstransport die veel gevoeliger is voor de aangebrachte gate spanning. Andere voorbeelden zorgen er juist voor dat de verandering van de gate sneller doorwerkt op de potentiaal van het kanaal. Als je dit vergelijkt met de waterkraan, dan is het net alsof je de kraan sneller kunt opendraaien. In dit proefschrift introduceren wij een concept om invloed van de gate spanning op het kanaal te versterken.

Recent is de zogenaamde FinFET in massaproductie genomen. Dit is een vinvormige transistor waarbij de gate om de hele vin gevouwen is. Daardoor heeft de gate een heel goede controle over het kanaal, en juist daardoor is dit type transistor in staat een subthreshold swing dicht bij de theoretische limiet van de conventionele transistor te halen.

In zulke transistoren wordt ook rek (mechanische uitrekking) gebruikt om de mobiliteit van de ladingsdragers te verhogen. Ze kunnen zich dan makkelijker door het kanaal verplaatsen, waardoor de maximale stroom toeneemt. In dit proefschrift bestuderen we transistoren gefabriceerd bij NXP-TSMC Research. Deze hebben een titanium-nitride (TiN) gate welke

bij een hoge temperatuur om de silicium vin gelegd is. Tijdens het afkoelen krimpt de TiN gate sneller dan het silicium, wat resulteert een negatieve rek (compressie) van het silicium. De hoeveelheid rek hangt af de relatieve volumes van het TiN en silicium. U kunt zich voorstellen dat een heel dikke silicium vin moeilijker in elkaar te drukken valt met een hele dunne laag TiN en vice versa. Daarom hebben de dunnere FinFETs over het algemeen een hogere rek.

Deze rek verandert behalve de mobiliteit ook de elektronenaffiniteit. Dit resulteert ook in een toename in de lekstroom. Gebaseerd op dit verschijnsel introduceren we in dit proefschrift een nieuw concept: een transistor waarin de rek schaalt met de aangelegde spanning. Dat betekent dat als de transistor aangezet wordt, de stroom nog verder toeneemt doordat de mechanische rek groter wordt.

Om zo een spanningsafhankelijke rek te krijgen stellen we voor een piëzoelektrische laag te gebruiken. Een piëzoelektrische laag zet uit onder invloed van de aangebrachte elektrische spanning. Door de FinFET tussen twee van zulke lagen te klemmen, en de gate spanning van de FinFET op de piëzoelektrische laag aan te sluiten ontstaat een transistor die gecomprimeerd wordt als hij aangezet wordt. Daardoor wordt tijdens het aanzetten de drempelspanning verlaagd waardoor de subthreshold swing nog kleiner wordt. Met behulp van elektrische en mechanische simulaties laten wij zien dat een subthreshold swing van 50 mV/dec bij kamertemperatuur haalbaar is, en dat is 9 mV/dec beter dan de thermische limiet.

In een mechanische rek gemoduleerde transistor is materiaalkeuze niet eenvoudig. Benodigd zijn zowel een piëzoelektrische laag die een grote druk kan uitoefenen op de vin, evenals een halfgeleider waarvan de elektrische eigenschappen sterk afhangen van de druk. Bovendien dient er ook een structuur gebruikt te worden die zorgt dat de beoogde materiaaleigenschappen op een efficiënte manier gebruikt worden.

Het uiteindelijke doel van de rek gemoduleerde transistor is een lager energieverbruik. De rek is proportioneel met de aangelegde spanning. Iedere keer dat de transistor aangezet wordt moet de rek opnieuw opgebouwd worden, dit kost energie en daarom neemt het zogenaamde dynamische energieverbruik van de transistor toe. Voordelig echter is de lagere lekstroom, en het daarbij behorende lagere statische energieverbruik. Het hangt dus van het verhouding tussen het statische en dynamische energieverbuik van de schakeling af of het moduleren van de rek zin heeft.

Contents

CHAPTER 1

INTRODUCTION

In recent years electronics have become the plastic of the 21st century, they have become integrated into everything. The result of this seamless integration is smarter products. Contrary to plastics, electronics do need power to operate. Whether it is your phone, car, or flashlight, you would be better off if the batteries lasted a bit longer. This is exactly to what this thesis hopes to contribute: proposing an alternative method to reduce the power consumption of the fundamental building block of all smart electronics: the transistor.

1.1 The FinFET

Since the invention of the basic transistor progress has been made to improve the performance of the transistor. Downscaling, the use of alternative materials, and the use of different transport mechanisms have all contributed to an improved device performance.

The transistor most recently introduced in production [1] is the FinFET or Tri-gate transistor [2, 3], here our discussion starts. A schematic of the FinFET is shown in figure 1.1. This fin shaped device is very well comparable to metal oxide semiconductor field effect transistor (MOSFET), however, the channel is surrounded by the gate, and lowly doped. Hence there is a negligible amount of fixed charge in the channel resulting in an improved control of the gate over the channel potential.

In figure 1.2 measured transfer characteristics of a FinFET are shown. Due to the almost perfect control of the gate over the channel the device has a subthreshold swing (SS) close to 60 mV/dec at room temperature, which is the theoretical limit for these devices [4]. Even when the gate voltage is zero a very small leakage current can be observed. A modern integrated circuit (IC) may contain up to a billion transistors. Multiply this number with the leakage current and the overall leakage current in

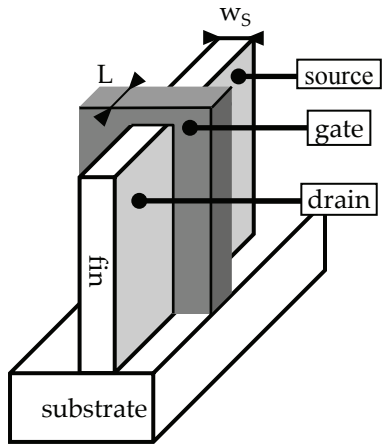


Figure 1.1: Schematic view of the FinFET.

an IC can be very large. This leakage current induces a static power consumption of the IC, which is becoming more and more important [5]. The static power consumption can be reduced by a lower leakage current. This could be realized by a higher threshold voltage. Unfortunately this requires also a higher supply voltage for an equal on current, which in turn increases the dynamic power consumption, the power required to switch the state of the transistor. To reduce the power consumption of an IC, without increasing either the static or the dynamic power consumption, a transistor with a smaller subthreshold swing is required. This can deliver a lower static power consumption, while maintaining a good on-current for a given supply voltage. Due to its enhanced gate control the FinFET already has the lowest possible subthreshold swing for a conventional transistor. Therefore novel transistors are being researched.

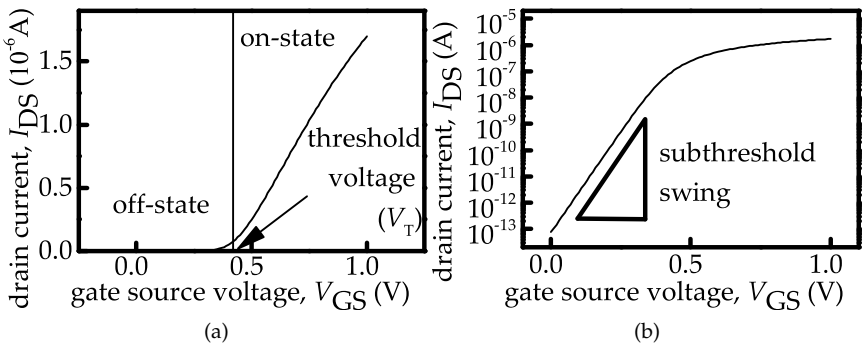


Figure 1.2: Measured drain source current as a function of the gate source voltage. The characteristics are shown on both (a) linear and (b) semi-log scale. This example is a measurement of the FinFETs from chapter 2.

1.2 Small subthreshold swing concepts

Some forms of alternative transistors have the same mode of charge transport through the device, however, the gate controls the channel potential in a different way.

An example is the negative capacitance transistor. Here the gate dielectric is supplemented with a ferroelectric layer. The non-linear voltage dependent charge in the ferroelectric layer is claimed to result in a smaller subthreshold swing [6, 7].

Another example is the suspended gate transistor [8]. In this device the gate dielectric includes both an oxide and an air gap. As the device is turned on, the air gap becomes smaller and hence the gate control of the channel potential is enhanced.

Unfortunately, in both concepts the transistor state tends to depend on the previous state. In other words, these devices show hysteresis.

Alternatively, an altogether different mode of charge transport could be chosen. This is done in the impact ionization transistor [9]. Here the current originates from the avalanche effect, which is strongly field dependent, and hence can result in a smaller subthreshold swing. To our knowledge impact ionization FETs with a reliable behaviour have not yet been reported.

Another concept is the band to band tunnelling transistor [10–12], where a smaller subthreshold swing results from the strongly electric field dependent band to band tunnelling process. These devices do show a small subthreshold swing, however, so far devices which also show a large on-current have not been reported [11].

1.3 Outline of the Thesis

In this thesis we contribute to the growing collection of small subthreshold swing concepts by changing the way in which the gate controls the channel potential. In a fully depleted long channel FinFET the subthreshold current [13], (see equation (2.6) on page 18), can be described as

$$I_{DS} \propto \exp\left[\frac{\chi_S - \phi_m + V_{GS}}{u_t}\right]$$

where u_t is the thermal voltage, χ_S is the electron affinity; the additional energy an electron in the conduction band requires to escape from the conduction band, and ϕ_m is the metal work function; the energy electrons require to escape from the metal. If the electron affinity χ_S could depend on the applied bias V_{GS}, than this would result in an additional change of the current I_{DS} as a function of the applied bias V_{GS}, and hence possibly a smaller subthreshold swing.

It has been shown that the electron affinity χ_S changes [14] with mechanical strain. In chapter 2 the dependence of the electron affinity on

the thermally induced strain and the fin width is studied. It is found that a negative strain results in a larger subthreshold current. Hence, if the strain could increase with the applied bias, then this would give a smaller subthreshold swing.

This voltage dependent strain can be introduced by a piezoelectric layer. In a piezoelectric material electric dipoles are present. When they are subjected to an electric field the dipoles displace resulting in strain.

It has been shown that a substrate strained with a piezoelectric layer can modulate the on-current of transistors [15]. We elaborate on this concept, however, propose in chapter 4 to add an individual piezoelectric layer to each transistor. This layer induces strain, which increases the electron affinity χ_S, which in turn increases the subthreshold current. Hence we can use the piezoelectric layer as an electric gear box to obtain a smaller subthreshold swing for each transistor individually.

A similar concept is the piezoelectronic transistor [16]. This device combines a piezoelectric layer and a piezoresistive material to obtain a transistor. Here the current is modulated in an unconventional material, while we modulate the current in the commonly used FinFET.

In chapter 3 we measure the parameters of a piezoelectric layer in a Bulk Acoustic Wave (BAW) resonator. We show that when a static electric field is applied to a resonator the resonance frequencies change. It is found that the bias induces strain and modifies the piezoelectric constants slightly. We introduce a simple method to extract the second order parameters from these changes.

Background information regarding the calculation of stress and strain in various materials can be found in appendix A. The exact coupling between the strain and the electron affinity χ_S and other band parameters of various semiconducting materials is shown in appendix B. The required parameters, and a list of all the constants, can be found in appendix C.

CHAPTER 2

STRAIN IN FINFETS

Currently the fin shaped field effect transistor (FinFET) is on its way to become one of the major workhorses in integrated circuits (ICs). Several techniques which have been used to increase the performance of the metal oxide semiconductor field effect transistor (MOSFET) are also applied to the FinFET; such as high-k dielectrics to enhance the gate capacitance, while maintaining a relatively low leakage current, mechanical strain to boost the charge carrier mobility, and downscaling to decrease the costs have been implemented in FinFETs.

This chapter investigates the influence of both strain and downscaling on the leakage current. Parts of the chapter have appeared in [TvH:5] and [TvH:8] . The effect of the strain on the mobility has been investigated [17]. We elaborate on this work by extracting the band offset [18] from the subthreshold characteristics, and investigate the strain dependence on the fin width.

We obtained highly scaled and strained FinFETs from NXP-TSMC Research, Leuven, Belgium [19] and measured their leakage characteristics. Section 2.1 discusses the amount and orientation of the strain in these devices. In section 2.2 we discuss how the very narrow body affects the band structure. Then, in section 2.3 the effects of both the small dimensions and the applied strain on the leakage current are discussed and a method to characterise this effect is described. In section 2.5 the method and theory are applied to the measured devices and in section 2.6 we present our conclusions.

2.1 Strain modelling

Figure 2.1 shows a schematic representation of the FinFET. The fin has source and drain connections and the channel region is surrounded by a dielectric and a gate. We investigated two differently oriented FinFETs.

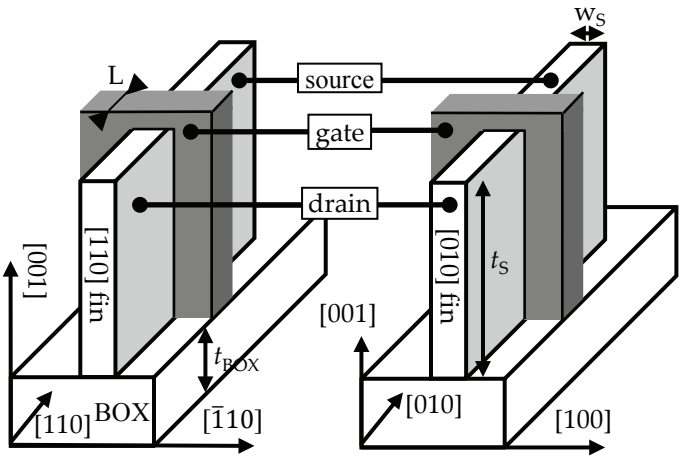


Figure 2.1: A schematic view of the [110] and [010] oriented FinFETs. The 65 nm high fin is on top of a 145 nm thick BOX layer. The surface orientation of the silicon wafer is [001], w_s is the fin width and t_s is the fin height.

The first has a [110] channel transport direction and $(1\bar{1}0)$ oriented sidewalls. The second has [010] as the transport direction and (100) oriented sidewalls. Figure 2.2 illustrates the 45 degree angle between the two different fins, from which the difference in orientations results. Note that the crystal coordinate system is also indicated.

The 65 nm high silicon fins measured in this work, see figure 2.3, are covered by a stack of 1 nm thick silicon dioxide (SiO_2) and 1.7 nm thick high-κ hafnium silicate (HfSiO) [19]. The composition is $Hf_{0.4}Si_{0.6}O$. On top of these the 7 nm thick titanium-nitride (TiN) and 100 nm thick poly-

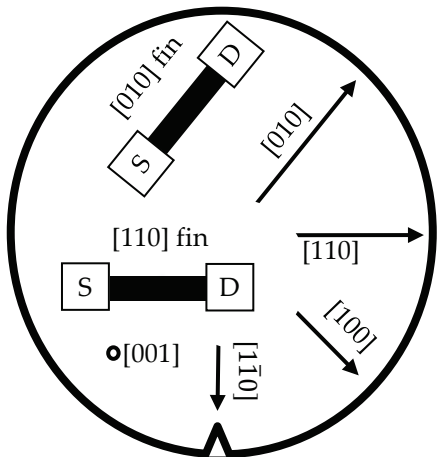
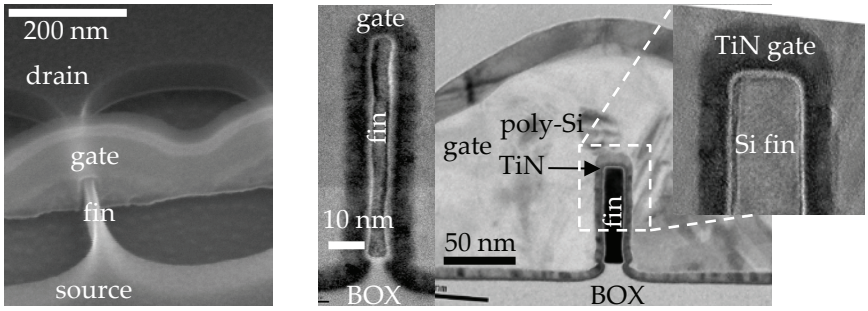


Figure 2.2: Schematic top view of a wafer with both [110] and [010] oriented FinFETs.

silicon (poly-Si) gate layers were deposited. During the front-end-of-line device integration of the FinFETs the gate underwent heat treatments as high as 1370 K. At these high temperatures the silicon channel deforms plastically and thus the strain relaxes [20]. When cooled down materials typically shrink. This is described by the coefficient of thermal expansion (CTE), which gives the relative change in the dimensions as a function of the temperature. For the materials used in this work this coefficient is shown in table C.6 on page 83. The TiN gate has a larger CTE than the silicon gate, when cooled down the TiN gate shrinks faster than the silicon fin. Hence the gate compresses the fin and a stress field is built up.



(a) (b)

Figure 2.3: TEM photos of FinFETs very similar to the devices used in this work. (a) Bird's eye view, (b) cross-sectional image. *These photos are printed with courtesy of Mark van Dal, TSMC Research.*

We investigated the plastic relaxation of the gate stack and subsequent stress build-up by implementing a multiphysics 3D finite element method (FEM) simulation [21] of the thermal expansion. We simulated the structure as shown in figure 2.1. To manage the computational load of the model we assumed the following.

We neglected the silicon substrate below the BOX layer, and applied fixed boundaries to the bottom of the BOX layer to mimic the stiff silicon substrate.

We verified that the results are essentially insensitive to variations of the BOX layer thickness, and thus simulating the complete substrate is not imperative. We simulated various degrees of corner rounding and found that this hardly affects the final result and hence rounding can be neglected as well.

The fins always form a group of five parallel fins, with a pitch of 200 nm between the centres of the fins. This configuration is simplified by simulating only one of the five fins and applying symmetric boundary conditions to the sides.

The step-coverage of the poly-Si has not been taken into account, however, we verified that the results are insensitive to thickness variations, which suggests that the step coverage is not relevant.

To mimic the behaviour of the relatively large and hence stiff source and drain connections the silicon fin was simulated 100 nm longer than the region overlapped by the gate, and symmetric boundary conditions were applied to the source and drain sides. All other boundaries are set free to move.

The parameters for the FEM simulations are summarized in table C.6 on page 83. An anisotropic model, as discussed in appendix A.2, was used for the silicon fin, while the other materials are modelled isotropically. Since HfSiO is a relatively unknown material its properties have not been determined with good precision. Furthermore, the literature references for the mechanical properties are obtained from bulk samples, whereas our structures are in the nanometre scale and hence the properties may be different.

The induced strain depends strongly, but not exclusively, on the CTE. For example, a material with a low stiffness is easier to deform and thus will receive a higher amount of strain.

To indicate the strain in these devices the Voigt notation is used, this is explained in section A.1 on page 65. The effect of strain on the crystal structure is shown in figure A.1. A strain along the [100] axis is labelled ε_1, along [010] ε_2, and along [001] ε_3. The deformation of the material along the [011] axis is labelled ε_4, along [101] ε_5 and along [110] ε_6, which are the shear strain components. The normal strain components convert the cubic unit cell into a rectangular box, while the shear strain components convert the cube into a parallelepiped.

Figure 2.4 shows the simulated strain components along the crystal axes of the 10 nm wide fin. Additionally the shear strain components are shown in figure 2.5. It can be observed that the strain is non-uniform and not equal for the two fin orientations. This has various reasons.

The thermal shrinkage of the gate metal compresses the fin surface in plane with the dielectric. For the [110] oriented fin this means compressive strain ε_3 and ε_6 at the sidewall interfaces and compressive strain ε_1 and ε_2 at the top interface. In the [010] oriented fin the picture is much more intuitive. The sidewalls have compressive strain ε_2 and ε_3, and the top a compressive strain ε_1 and ε_2.

The silicon fin and gate stack are fabricated on top of a BOX layer. The oxide has a much smaller stiffness compared the silicon fin, see table C.6 on page 83. Therefore the BOX cannot act as a stressor and so the bottom of the fin is relatively relaxed.

The dielectric layers surrounding the silicon fin, being SiO_2 and HfSiO, have a relatively low stiffness. Therefore they deform much more than the silicon fin under stress, this explains the larger absolute strain levels in the dielectric.

The dimensions of the various layers have an influence on the uniformity and scale of the strain in the silicon fin. As these dimensions vary for the different axes non-uniformities are to be expected. From holographic

interferometry measurements [22] we expected a strain along the [001] axis of ε_3 = -0.8%, which in fact is comparable with the silicon volume average of the simulated strain as shown in figure 2.7.

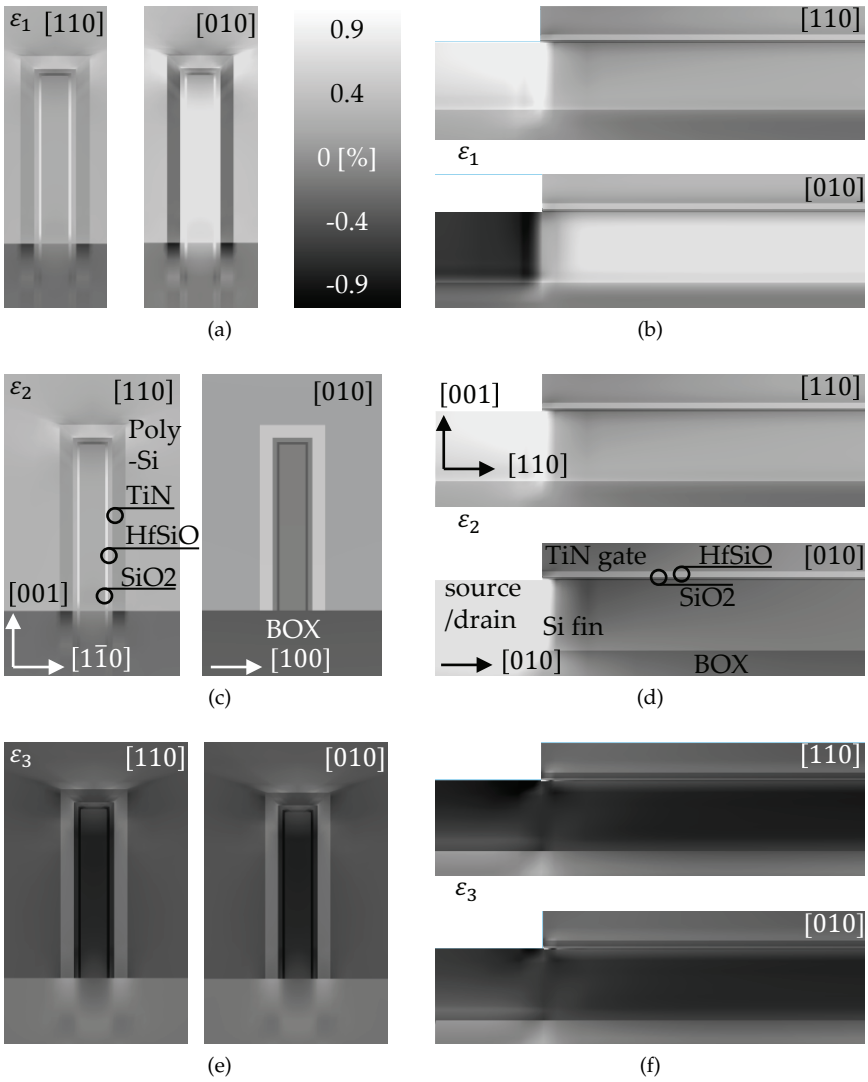


Figure 2.4: Cross sectional views of the fin showing the simulated strain at room temperature for a 10 nm wide fin. Note that the crystal coordinate axes are indicated. (a,c,e) show the strain on cross-section through the fin along the width, while (b,d,f) show the strain on a cross-section along the length of the fin.

In the simulation elastic deformation, i.e. a linear relation between the stress and strain, has been assumed. This holds as long as the strain is well below the elastic limit of the materials. These limits are shown in table C.6 on page 83. To our best knowledge the elastic limit for HfSiO has not yet

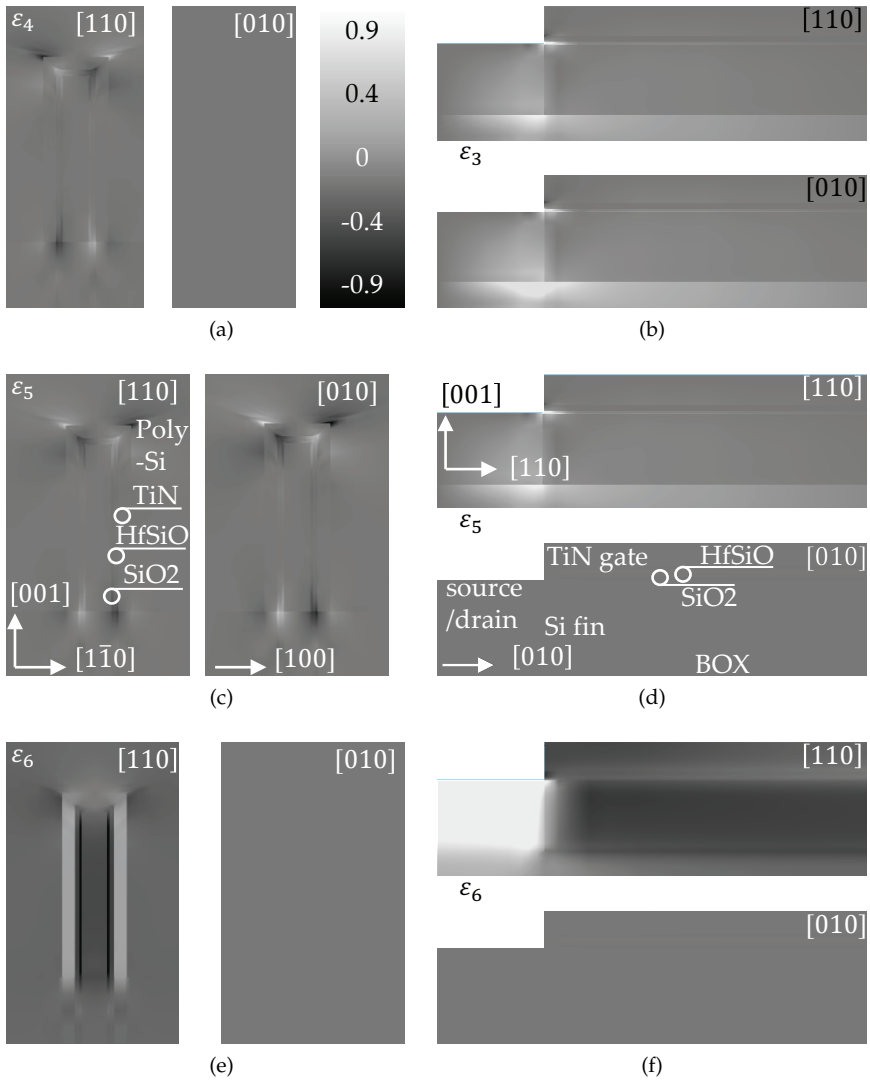


Figure 2.5: Cross sectional views of the fin showing the simulated shear strain at room temperature for a 10 nm wide fin. (a,c,e) show the strain on cross-section through the fin along the width, while (b,d,f) show the strain on a cross-section along the length of the fin.

been published. For the other materials we found maximum strain levels well below this limit.

In this work, we aim to model the band offset as a function of the strain and fin dimensions. The simulations show a slightly non-uniform strain. From which we calculated the resultant non-uniform current. We found a 1% change in the current ratio between a wide and narrow FinFET. This non-uniform strain effect can therefore be neglected and uniform strain can be assumed. In the remainder of the chapter when we mention strain,

we refer to the average strain in the silicon fin surrounded by the gate.

As mentioned before, the strain is a result of a difference in CTE between materials. Hence it can be insightful to simulate the strain as a function of the temperature. This is shown in figure 2.6. Remember that at 1370 K plastic relaxation is assumed, and hence the strain is then zero. When cooling down the strain increases. Therefore the strain will also change over the temperature range used for the electrical measurements. The graph shows that the strain varies about 0.1% with the temperature used in our electrical measurements. Nevertheless, this 0.1% change is relatively small compared to the overall strain of -0.6%.

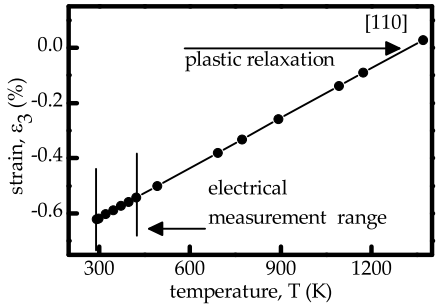


Figure 2.6: Simulated strain in a 10 nm wide fin as a function of the temperature. The high density of points around room temperature indicates the electrical measurement range.

In addition, the fin width dependence of the average strain in the fin, after the cool-down step introducing strain, has been investigated. In figure 2.7 (a) an absolute increase of ε_3 and ε_6 with smaller fin width can be observed. This can be explained by the fact that the sidewalls are compressed along [001] and along [110]. Hence for smaller fins more of the fin volume is closer to the sidewalls, resulting in larger average strain values. Alternatively one could say that for smaller fins the relative volume of silicon becomes smaller and hence the strain larger. For the [010] oriented fins the same holds. In figure 2.8 (b) strain components ε_1 and ε_3 become larger for smaller fins, resulting from the increased influence of the strain from the sidewalls.

Compared to the holographic interferometry measurements [22] the simulated strain is in the same order, however, shows a weaker dependence on the fin width. Therefore we use the FEM results only to estimate non-measured strain components and to inter- and extrapolate the strain for non-measured fin widths.

Estimating the strain ε_3 in figure 2.7 (a) for an infinite fin width results in close to zero strain, this is explained by the fact that the lateral interfaces are an infinite distance away, and hence they cannot compress the fin along the [001]-axis. On the other hand, a zero fin width cannot result in infinite strain and hence should give a maximum. This behaviour can

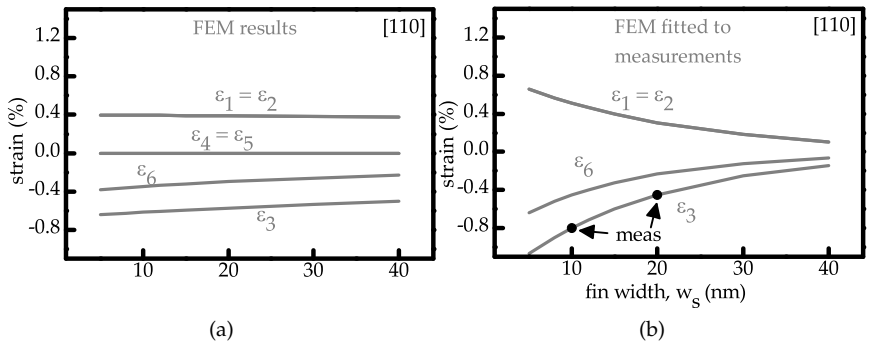


Figure 2.7: (a) Strain dependence on the fin width as obtained from the FEM simulations. (b) Strain, obtained from FEM simulations and corrected to the holographic measurement data [17]. Both graphs are at room temperature.

be fitted well with an exponential function.

In our earlier work [TvH:5] we assumed a linear dependence, however, a linear function cannot fit the strain for a zero fin width and zero strain for infinite large fin width.

The holographic interferometry measurements [22] are available only for two fin widths and orientations, however three data points are needed to fit an exponential function. Therefore we add a third point to the measurements with w_s = 1000 nm and $\varepsilon_3 = 0$.

To calculate the effect on band alignment and quantum confinement the complete six component strain tensor is required for all fin widths. To estimate this tensor we extract the ratio of the components of the strain tensor, for instance $\varepsilon_6/\varepsilon_3$, from the simulations. These ratios multiplied

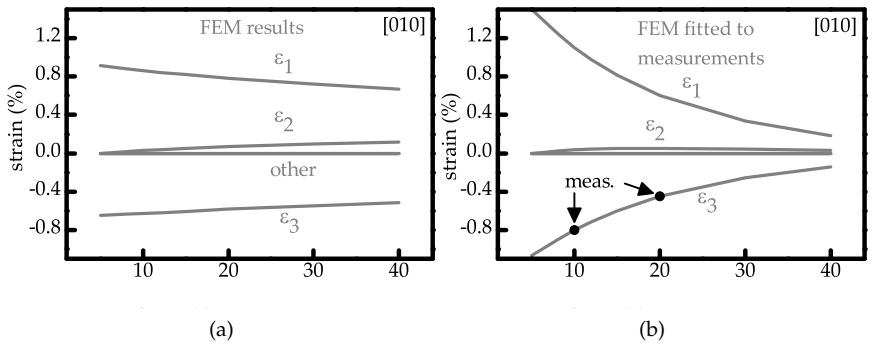


Figure 2.8: (a) Strain dependence of the fin width as obtained from the FEM simulations. (b) Strain, obtained from FEM simulations and corrected to the holographic measurement data [17]. Both graphs are at room temperature.

by the measured and extrapolated data for ε_3 give a good approximation for the complete strain tensor for all considered fin widths. This approach can be justified by all stress-strain relations being linear. This procedure has been followed for both [110] and [010] oriented fins.

The corrected strain which has been exponentially fitted to the measurement points is shown in figure 2.7 (b) and 2.8 (b). Fitting the simulated data to the holographic interferometry measurement data for ε_3 resulted in a stronger dependence of the strain on the fin width. In the rest of the chapter these inter- and extrapolated values will be used for further calculations.

2.2 Quantum Confinement

It has been reported that the conduction band valleys in a semiconductor depend on strain [14, 23, 24]. However, there is an additional effect to take into account. If an electron is seen as a particle then there is some uncertainty or fluctuation of the exact position of the particle. This fluctuation is described by the de Broglie wavelength and can be calculated, which is a measure of the position uncertainty of the electron.

For example an electron in bulk silicon at room temperature can easily have an energy of $k_B T$ above the conduction band, resulting in a de Broglie wavelength of 7.7 nm. Very narrow fins may have silicon dimensions close to this wavelength. However, the electron is confined to positions inside the silicon, resulting in a coupling between the dimensions of the silicon fin and the allowed energy levels of the electron.

The allowed energy levels can be derived from quantum mechanics. The electron is described by a wave function Ψ. In our case this wavefunction has to be a solution to the time-independent Schrödinger equation [25]

$$\frac{\partial^2 \Psi}{\partial^2 w} + k_w^2 \Psi = 0 \qquad \text{with} \qquad k_w^2 = \frac{2 m_{w,k} E}{\hbar^2} \tag{2.1}$$

where w is the position along the width of the silicon fin, $\hbar$ is the reduced Plank constant, E is the energy of the electron, $m_{k,w}$ is the quantization effective mass of valley k in direction of w, and k_w is the corresponding electron wave number. A general solution to the time independent Schrödinger equation along w is given by

$$\Psi(w) = A \sin(k_w w) + B \cos(k_w w) \tag{2.2}$$

where A and B are constants. In our study the silicon body is viewed as a square potential well as shown in figure 2.9.

In a fully depleted FinFET operated in the subthreshold regime the number of charge carriers is low, hence all the carriers will occupy the lowest energy levels available, given by equation (2.4). This is a defendable approximation in the subthreshold regime we are mostly interested in (see section 2.4) because the electric fields in the subthreshold regime

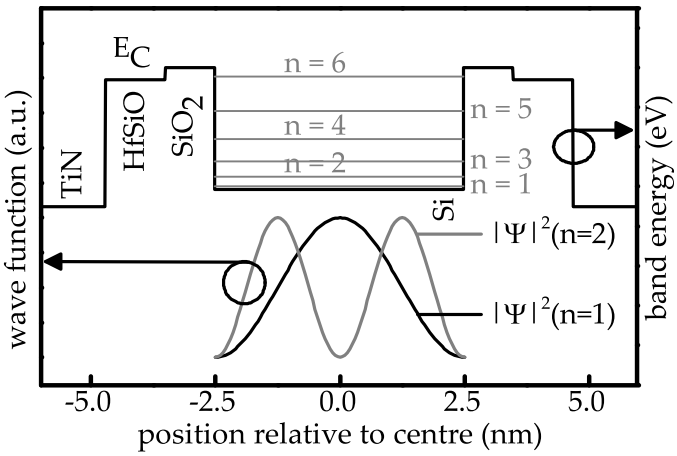


Figure 2.9: Schematic showing the potential well and electron probability function $|\Psi|^2$. The graph also shows the conduction band along a cross section through the device, including the quantization energy levels $E_k(n)$ for a 5 nanometre wide fin.

are relatively small. Hence their influence on the shape of the potential well can be neglected.

For the sake convenience the well is assumed infinitely deep, it has been shown that this assumption holds for fin widths down to 5 nm [18]. In an infinitely deep well the electron wavefunction cannot reside outside the silicon body, resulting in a confined movement of the electron in the w direction. This effect is termed quantum confinement [26]. Confinement means that the electron wave function is limited to the quantum well. We assume an infinite deep quantum well, hence the wave function has to be zero outside the quantum well, yielding the boundary condition $\Psi(0) = \Psi(w_s) = 0$, therefore $B = 0$ and

$$\Psi(w) = A \sin k_w w \qquad \text{with} \qquad k_w = \frac{n\pi}{w_s} \tag{2.3}$$

where integer n runs from zero to infinity. This means that the wavefunction Ψ has to fit an integer times into the silicon body. This results in quantization of the wavenumbers available to k_w, as is shown in figure 2.9. The extra energy required due to the quantization is given by

$$E_k(n) = \frac{\hbar^2}{2m_{k,w}} \left(\frac{n\pi}{w_s}\right)^2 \tag{2.4}$$

an electron residing in the silicon quantum well thus has to have an extra energy $E_k(n)$ to fit into the quantum well. As a result energy levels below this energy are now forbidden and the bandgap effectively widens.

Table 2.1: Parameters used for band deformation calculation from [14]. The quantization masses [26] are expressed in the electron rest mass (m_0) and given separately for each of the conduction band Δ valley pairs.

Ξ_d[eV]	Ξ_u[eV]	Θ	η	κ
1.1	9.29	0.53	-0.809	0.189

orient.	w dir.	$m_{\Delta_{[100]},w}$	$m_{\Delta_{[010]},w}$	$m_{\Delta_{[001]},w}$
[110]	$[\bar{1}10]$	0.315	0.315	$0.19(1+\eta\varepsilon_6/\kappa)^{-1}$
[010]	[010]	0.916	0.19	0.19

2.3 Band Offset Theory

In the previous section the offset of the conduction band valleys due to the quantum confinement was described, however, strain also affects the position of the bands. In appendix B this dependence is described using the Bir and Pikus model. Both quantum confinement and strain have an influence on the conduction band. We assume that the total offset of the valleys can be estimated by the superposition of the offsets due to strain as shown in equation (B.3), and quantum confinement as shown in equation (2.4). In figure 2.7 and 2.8 it can be observed that the shear strains ε_4 and ε_5 are zero, hence we simplify matters by not showing the dependence on these terms. We find

$$\begin{aligned} E_{\Delta_k}(\varepsilon, n) &= E_{\Delta_k}(\varepsilon) + E_k(n) = \Xi_d^{\Delta}(\varepsilon_1+\varepsilon_2+\varepsilon_3) \\ &\quad + \Xi_u^{\Delta}\varepsilon_k + E_{\Delta_k}^{\text{shear}} + \frac{\hbar^2}{2m_{k,w}}\frac{n^2\pi^2}{w_s^2} \\ E_{\Delta_{[001]}}^{\text{shear}} &= -\frac{\Theta}{4\kappa^2}\varepsilon_6^2 \end{aligned} \tag{2.5}$$

where k = [100], [010], [001] is the valley index, the $\Delta_{[100]}$ valley corresponds to electrons with a large momentum in [100] direction, $\Delta_{[010]}$ to those in [010] direction and $\Delta_{[001]}$ to those in [001] direction, and n is the subband index. Ξ_d and Ξ_u are the deformation potentials, in this case for silicon Δ valleys, Θ and κ the model parameters from [14], whose numerical values are summarized in table 2.1, and η is a model parameter. $E_{\Delta_k}^{\text{shear}}$ is shown for the k = [001] valley only. It is zero for the [100] and [010] valley because ε_4 and ε_5 are both zero. Hence, it is not necessary to show the shear strain dependence for the other valleys. The same holds also for the dependence of the quantization effective masses.

The only non-zero shear strain component is ε_6. In the [110] fins this strain changes the quantization mass $m_{\Delta_{[001]},w}$ slightly. Note that the mass also depends on the valley index.

The dependence of the effective masses and valley pairs on the applied strain can be illustrated by drawing the various vectors of momentum which an electron can have for a given energy above a reference energy.

The total energy of the electron is derived from the sum of the energies in all three directions, see equation (B.1). Generally the minimum of the

valley is used as a reference [26]. However, we would like to illustrate the larger occupation of a certain valley if it is shifted down due to strain. Hence we use the lowest conduction band valley pair as a reference and plot the equi-energy surfaces for 0.5 eV above this valley.

The other valley pairs may have a higher minimum and hence the equi-energy surface is plotted for an energy lower than 0.5 eV, resulting in smaller equi-energy surfaces. The result is shown for both a relaxed fin and for the highly strained 5 nm wide fin in figure 2.10.

In the relaxed case the valley pairs are degenerate and hence the equi-energy surfaces are symmetrical. Their shape is ellipsoidal and from the dimensions the effective masses can be derived. The ellipsoids are relatively long along their corresponding axis, for example the ellipsoid of the $\Delta_{[100]}$ valley is relatively long along $k_{[100]}$ and hence has a large effective mass along this direction. This mass is called the longitudinal mass. The masses which describe the dimensions along $k_{[100]}$ and $k_{[010]}$ of the $\Delta_{[100]}$ ellipsoids are called the transverse masses which are much smaller.

The quantum confinement effect in the [010] FinFETs is along the [100] direction, see also figure 2.1, hence the quantization effective mass as shown in table 2.1 is given by the dimension of the corresponding valleys in the $k_{[010]}$ direction.

For the [110] oriented FinFETs matters are more complicated. There is also a shear strain ε_6 present, this changes the shape of the $\Delta_{[001]}$ valley ellipsoid, which in turn is a change of the effective mass, see also equation B.4. The shear strain ε_6 is small and negative and hence the mass along [001] increases. The ellipsoids become scalene in the (001) plane (the plane along [100] and [010]), the mass along [110] becomes smaller and along $[\bar{1}10]$ becomes larger. This is also illustrated in figure 2.10. The quantization of the [110] FinFETs is along $[\bar{1}10]$ and grows with applied negative shear strain ε_6.

In addition the strong compressive strain ε_3 moves down the $\Delta_{[001]}$ valley pair, and hence the equi-energy surface, drawn with the lowest of the valley pairs as a reference, logically becomes the largest for the reference valley. As a result the ellipsoids drawn in figure 2.10 are the largest for the $\Delta_{[001]}$ valleys.

The quantum confinement effect strongly depends on the effective mass, which was illustrated in figure 2.10. The total energy offset of the conduction band valleys is given by the offset due to strain and quantum confinement. In figure 2.11, the energy offsets for the lowest subbands of the three conduction band valleys are shown as a function of the fin width. To ease comparison with results presented further on in this chapter, the 30 nm fin width is taken as a reference for the [110] and the 40 nm fin width for the [010] oriented fins.

The strain leads to a splitting of the conduction band valleys. With compressive strain ε_3 the $\Delta_{[001]}$ valleys move down and the other valleys move up. For [110] oriented devices the strain along the width and length

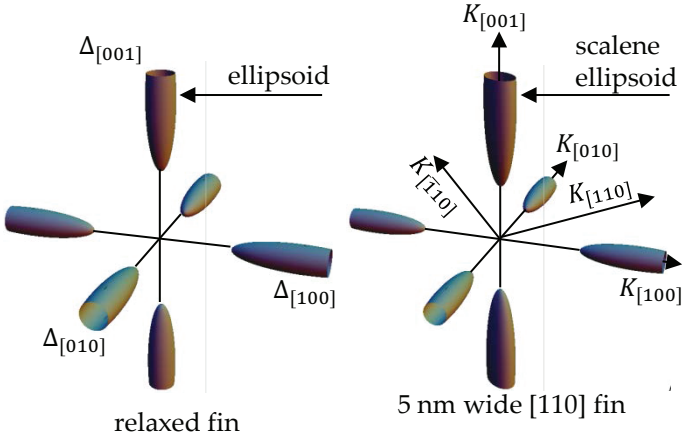


Figure 2.10: Equi-energy surfaces in the proximity of the conduction band Δ minima for a relaxed and highly scaled and strained FinFET. There are three Δ valley pairs located between the Γ and six X points in the reciprocal (momentum) space. The dimensions have been normalized to $[\frac{2\pi}{a_0}]$, where a_0 is the unstrained lattice constant. The equi-energy surfaces are still quite small and diffucult to see, therefore we magnified the ellipsoids around their center by a factor of three.

of the fin is shear to the crystal unit cell, and results in an equal strain ε_1 and ε_2, and a shear term ε_6, which result in an equal offset for both the $\Delta_{[100]}$ and $\Delta_{[010]}$ valleys. In the [010] channel, instead, the strain displaces the valleys differently.

For both cases the compressive strain ε_3 along [001] moves down the $\Delta_{[001]}$ valley pair. Most of the electrons occupy the lowest available subband. Therefore a measurement of the conduction band offset effectively probes these $\Delta_{[001]}$ valleys.

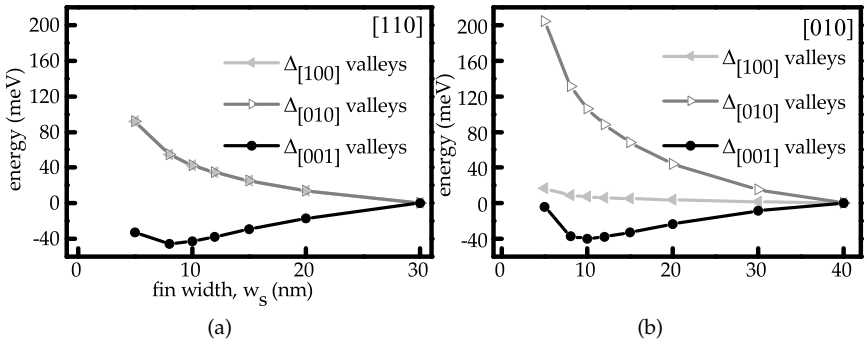


Figure 2.11: Calculated offset of the conduction band valleys due to strain and quantum confinement. (a) for the [110] oriented fins and (b) the [010] oriented fins.

Note that the substrate potential, which is the bias below the BOX layer in figure 2.1, can have an influence on the potential of the channel. This effect is characterized by the body factor [27]. For our devices, which have a BOX thickness of 130 nm, 65 nm fin height and 5-40 nm fin width, the body factor is below 1.0018 for 40 nm wide fins and 1.0004 for the 5 nm wide fin. This means that the capacitance between substrate and silicon fin is 0.0018 times the capacitance between the gate and the silicon fin. Therefore the effect of the substrate bias can be neglected.

In a narrow high aspect ratio undoped FinFET, the charge density in the subthreshold regime is fairly uniform along the fin width [28]. The electron gas is non-degenerate and hence the subthreshold current is given by [13]

$$\begin{aligned} I_{DS} =& N\frac{t_s \mu q u_t}{L}\left(1-\exp\frac{-V_{DS}}{u_t}\right)\exp\left(\frac{\chi_S-\phi_m+V_{GS}}{u_t}\right) \\ &\cdot\frac{k_B T}{\pi\hbar^2}\sum_{k,n} m_{d,k}\exp\left(-\frac{\min(E_{\Delta_k}(\varepsilon,n))}{k_B T}\right) \end{aligned} \tag{2.6}$$

where N is the number of parallel fins, L is the length of the channel, k_B is the Boltzmann constant, t_s is the fin height, μ the electron mobility, χ_S the electron affinity, ϕ_m the metal work function and $m_{d,k}$ the conduction band density of states effective mass. If, as assumed earlier, the lowest subband, in our case given by $k = [001]$ and $n = 1$, carries most of the current, then the subthreshold current ratio of devices with different fin widths yields

$$\eta_{rat} = \frac{I_{meas}}{I_{ref}} \propto \exp\left(\frac{\Delta E_{\Delta_{[001]}}}{k_B T}\right), \tag{2.7}$$

where I_{meas} and I_{ref} are the subthreshold currents obtained from a narrow fin and reference (wide) fin device respectively. The temperature derivative of η_{rat} gives the conduction band offset between the wide and narrow fin device.

One of the most important assumptions involved in this method is that the temperature dependence of the exponent in equation (2.6) is much stronger than the temperature dependence of the prefactor. Although the mobility and the density of states do change with temperature, only a difference in temperature dependence of the various fin widths can introduce an error in the extracted band offsets.

The influence of the prefactor can be verified by assuring that the subthreshold swing varies linearly with temperature, and has equal values for the whole fin width range. Furthermore, a different temperature dependence of the low field mobility on the applied strain is not expected [29].

2.4 Experimental Technique

The FinFETs were obtained from NXP-TSMC Research, Leuven, Belgium [19]. Temperature dependent transfer characteristics were recorded with a Keithley 4200-SCS parameter analyser and a Cascade probe station.

The temperature dependence of η_{rat} was used to calculate the conduction band offset [13]. The obtained results are valid as long as equation (2.6) holds, this can be verified from the temperature dependence of the extracted subthreshold swing, which should be almost the same for the considered fin widths in the considered temperature range. Moreover, the devices should not show short channel effect (SCE), which is in fact the case for the long devices used in the measurements.

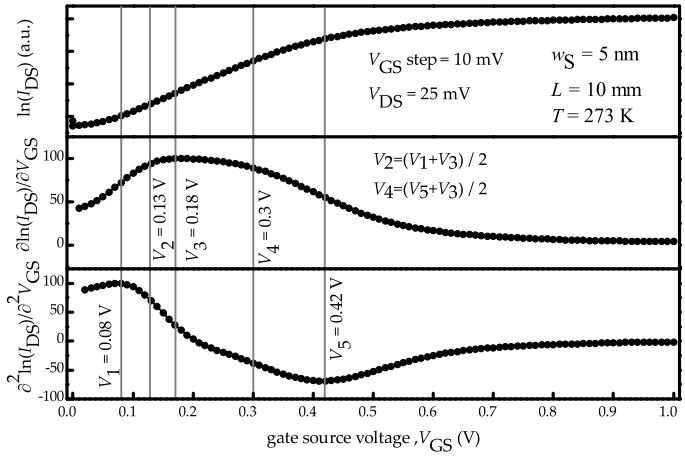


Figure 2.12: The $\ln(I_{DS})$ and smoothed derivatives as a function of the gate voltage which are necessary to define the subthreshold region of the graph. For the sake of convenience normalized values are used for the derivatives. The $\partial \ln(I_{DS})/\partial V_{GS}$ peak is located at V_3, the $\partial^2 \ln(I_{DS})/\partial^2 V_{GS}$ peaks at V_1 and V_5 respectively.

For further analysis, it is convenient to have a definition for the region where equation (2.6) holds, which we call the subthreshold region. In figure 2.12 a typical transfer characteristic is shown as $\ln(I_{DS})$. For very low voltages the current consists only of leakage current, for high voltages, where $V_{GS} > V_T$, the device is in strong inversion. In between is the subthreshold region. Here the current increases exponentially as a function of the gate source voltage V_{GS}.

Figure 2.12 also shows the normalized first derivative, $\partial \ln(I_{DS})/\partial V_{GS}$, and second derivative, $\partial^2 \ln(I_{DS})/\partial^2 V_{GS}$. The peak of $\partial \ln(I_{DS})/\partial V_{GS}$ at V_3 is in the centre of the subthreshold region. The maximum of $\partial^2 \ln(I_{DS})/\partial^2 V_{GS}$ at V_1 gives the beginning of the subthreshold region. Equivalently, the minimum indicates the end at V_5. Similar methods have been proposed to obtain the threshold voltage (V_T) at V_5 [30] or to characterize the hump

effect [31]. We define the lower and upper limit of the subthreshold region at V_2 and V_4 respectively.

$$V_2 = (V_1 + V_3)/2 \quad V_4 = (V_5 + V_3)/2 \tag{2.8}$$

An exponential function was fitted to the current in this subthreshold region. The fit gives the average subthreshold swing in the subthreshold region. From the fit the conduction band offset was extracted with the method described in section 2.3.

2.5 Band Offset Results

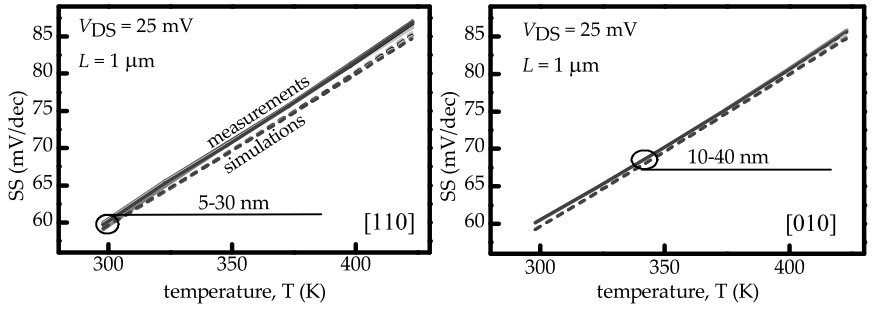


Figure 2.13: Extracted subthreshold swing of the FinFETs from both measurements (lines) and TCAD simulations (dashed lines). Shown for (a) [110] oriented fins, the devices with 5-30 nm fin width show a linear temperature dependence of the subthreshold swing and a small variation. Hence the CB offset can be calculated from the subthreshold characteristics. (b) The same for the [010] oriented fins. Here the 10-40 nm fin widths show suitable subthreshold swing.

The subthreshold region of the measured transfer characteristics was identified with the method shown figure 2.12. Extracted values for the subthreshold swing are shown in figure 2.13.

According to equation (2.6) the subthreshold swing of the considered fin widths should be the same. Clearly, this is the case for the fin widths shown in the figure. Hence we can use a 30 nm and 40 nm wide fin as a reference for the [110] and [010] orientation respectively. In addition, the subthreshold swing extracted from simulations [32] including band offset due to strain, and quantization effects using the density gradient model [33, 34], are shown. The results are in good agreement with the measurements.

We measure a current obtained from an ensemble of electrons, therefore any extracted parameter represents an average or effective value. With equation (2.7) the band offsets were extracted, and are shown in figure 2.14.

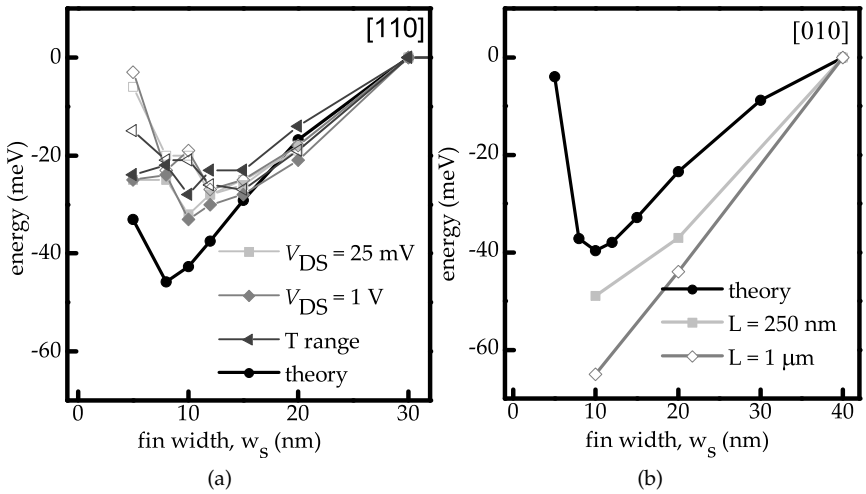


Figure 2.14: The extracted conduction band offset with the values according to the theory of the [001] valleys obtained from figure 2.11. The open symbols are for 1 µm long fins. (a) For the [110] oriented fins, where also results obtained with V_{DS} = 1 V instead of 25 mV, and results obtained with a smaller temperature range, from 293 instead of 233K, are shown. Closed symbols are for 10 µm long fins. (b) The same as for the [010] oriented fins, here the closed symbols are for 250 nm long fins.

The results reveal a lowering of the conduction band for smaller fin widths. Additionally, for the [110] orientation we have data for fin widths below 10 nm, where the conduction band starts to shift up. For comparison the calculated offset of the lowest conduction band valleys, in our case the $\Delta_{[100]}$ valleys, is also shown. Both theory and measurements show the same qualitative dependence on the fin width. Additional measurements were done with an alternate temperature range and V_{DS}. These show no qualitative difference. Therefore, the general observation is, that narrowing the fins increases the compressive strain, as predicted by FEM simulations fitted to measurement data, see figure 2.7 and 2.8. The increase of compressive strain shifts the $\Delta_{[001]}$ valleys downward. Fin widths below 10 nm were available for the [110] orientation only and here quantization needs to be taken into account. This effect counteracts the strain and in turn shifts the $\Delta_{[100]}$ valleys upward.

2.6 Conclusion

In this chapter we investigated the conduction band offset in narrow FinFETs. This offset is partly caused by strain. With FEM multiphysics simulations we simulated the build-up of strain due to difference in thermal expansion coefficients of the metal gate and the silicon fin, these showed the exact amount of strain also depends on the dimensions, elasticities of

both materials, and the interfacial layers. From the simulations we obtained the ratio of the different strain components. Applying this ratio to actual measurements of the most important strain component yielded an estimate of the complete strain tensor.

The conduction band offset was calculated as a function of the fin width and strain. The obtained calculations for both [110] and [010] oriented silicon fins are comparable with measured conduction band offsets. The conduction band offset can be explained by the superposition of two physical effects: (1) an increase in compressive strain in the fin height direction for narrower fins moving the conduction band $\Delta_{[001]}$ valleys downward: and (2) quantum confinement for fin widths below 10 nm, separating the energy levels available to electrons and moving the conduction band valleys upward.

Downscaling of the fin width involves a strain and quantum confinement effect on the effective conduction band edge. There is a certain fin width where the effect of the compressive strain and the quantum confinement become equally important. At this fin width small deviations of the fin width only result in a small change of the current. Hence at this fin width the two effects counteract each other which may be of interest to improve matching between devices which suffer from fin width variations.

CHAPTER 3

First and Second Order Piezoelectricity

The main objective of this thesis is the theoretical investigation of the performance of the strain modulated fin shaped field effect transistor (FinFET), which combines a piezoelectric layer and a narrow FinFET to obtain a low subthreshold swing device. Additionally, in chapter 2 we analyse and discuss the characteristics of the FinFET in the presence of strain. In this chapter we present a more fundamental research, based on experimental results, on the behaviour of piezoelectric materials.

This work started as an examination of the piezoelectric parameters by measuring the dependence of the capacitance on the applied electric field, which has been published earlier [TvH:4] . However, the resultant piezoelectric displacement parameters could not be matched to existing literature. The addition of resonance measurements allowed extracting the three piezoelectric parameters, elasticity, permittivity, and charge, independently [TvH:6] .

We start with a short discussion on Bulk Acoustic Wave (BAW) resonators, followed by the first and second order piezoelectric constitutive equations in section 3.2. In section 3.3 the model to fit the frequency characteristics of the resonators is shown. The devices are discussed in section 3.4 and the fitted piezoelectric parameters are shown in 3.6. In section 3.7 a method is introduced to reduce the number of independent second order piezoelectric parameters, of which the results are discussed in section 3.8. Finally in section 3.9 conclusions are presented.

3.1 Bulk Acoustic Wave Resonators

A typical application of a piezoelectric material is a BAW resonator. When an electrical sine wave is applied to a piezoelectric layer the layer will de-

form accordingly, resulting in an acoustic wave. If the acoustic wave is not absorbed, but reflected by the electrical contacts, and if this reflection is constructive with the electrically induced acoustic wave, then the piezoelectric layer starts to resonate. This minimizes the electric impedance and therefore the BAW resonator can be used as a building block for a frequency filter.

In this chapter BAW filters are used for the characterization of a piezoelectric material. The available resonators are targeted at GHz frequencies for filter applications in mobile communication.

Typical sound velocities are in the range of 3000–11000 m/s. Mobile applications require filters in the GHz range. Combining these numbers gives a wavelength in the micrometre range. The piezoelectric needs to have a thickness equal to approximately half the acoustic wavelength. Thicknesses in this range can be controlled accurately with modern microelectronic planar technology [35].

Figure 3.1 shows an example of a band-pass filter by combining two different BAW resonators: a series and a shunt, also called parallel, resonator. At the resonance frequencies the impedances are very small. At the anti-resonance frequency the electric field is anti-parallel to the polarization, as a result the piezoelectric is charged only minimally and hence the impedance is large.

The shunt resonator has a lower resonance frequency with respect to the series resonator. A maximum signal is transmitted when the resonance frequency of the series resonator equals the anti-resonance frequency of the shunt resonator. At the anti-resonance frequency of the series resonator the input is blocked. At the resonance frequency of the shunt resonator the impedance is small, effectively coupling the output to the ground. Hence the bandwidth of a filter is determined by the separation between resonance and anti-resonance frequencies of the two resonators.

3.2 Constitutive Equations

Accurate modelling is required to obtain a good understanding of the behaviour of BAW resonators. This starts with a model for the piezoelectric material. Therefore we recall the stress-charge form of the first order piezoelectric constitutive equation, see equation (A.4). In the devices measured in this work the lateral dimensions of 182 and 250 μm are very large compared to the thickness of the active layer, which is ≈ 1 μm, also shown in figure 3.2. Hence the displacement can be assumed one-dimensional along the polar axis only, by convention the [001] axis. The constitutive equations along this axis are

$$T_3 = c_{33}^E \varepsilon_3 - e_{33} E_3 + \Delta T_3 \tag{3.1a}$$

$$D_3 = e_{33} \varepsilon_3 + \kappa_{33}^\varepsilon E_3 + \Delta D_3 \tag{3.1b}$$

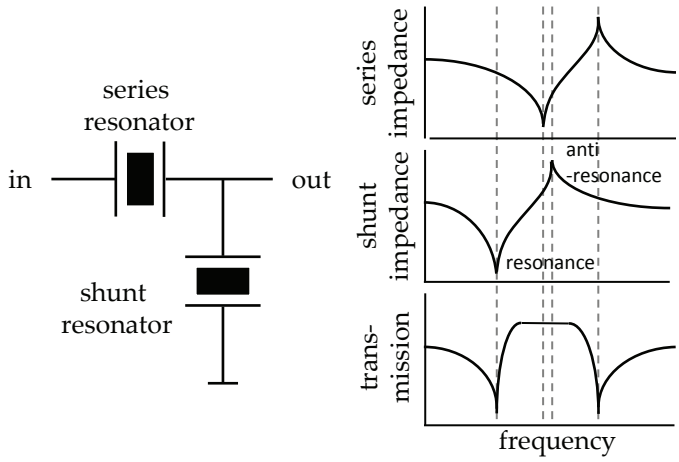


Figure 3.1: Schematic and frequency response of a BAW filter. The combination of a series and a parallel resonator, where the latter has a lower resonance frequency, results in a band-pass filter [35].

where the subscript $_3$ represents the polar axis [001], the piezoelectric parameters are c_{33}^E the stiffness, e_{33} the charge constant and κ_{33}^ε the dielectric constant. T_3 is the mechanical stress, ε_3 the strain, D_3 the dielectric displacement and E_3 the electric field. ΔT and ΔD are the nonlinearities in the equations for force and displacement.

It has been widely agreed upon that the nonlinearities stem from the nonlinear response of the piezoelectric layer [36]. For example a stress dependence of the stiffness, strain and electric field dependence of the dielectric displacement or strain dependence of the piezoelectric constant all have been modelled to accommodate the measured non-linearity. A more complete set, incorporating the second and third order piezoelectric response to accommodate the non-linearity was proposed by [36, 37]. The second order equations are

$$\Delta T_3 = \frac{1}{2}\delta_3 c_{33}^E \varepsilon_3^2 - \delta_1 e_{33}\varepsilon_3 E_3 + \delta_2 \frac{1}{2}\kappa_{33}^\varepsilon E_3^2 \tag{3.2a}$$

$$\Delta D_3 = \frac{1}{2}\delta_1 e_{33}\varepsilon_3^2 - \delta_2 \kappa_{33}^\varepsilon \varepsilon_3 E_3 + \frac{1}{2}\delta_4 \frac{e_{33}\kappa_{33}^\varepsilon}{c_{33}^E} E_3^2 \tag{3.2b}$$

There are four second order coefficients δ_i; δ_1 is the strain dependence of the piezoelectric charge constant, δ_2 the electric field dependence of the piezoelectric charge constant, δ_3 is the strain dependence of the bulk modulus, and δ_4 the electric field dependence of the dielectric constant.

Unfortunately, the second and third order equations together require nine parameters to be measured. These parameters can be estimated by measuring the second order harmonic and third order intermodulation distortion [36].

We developed a straightforward and accurate method to extract the four second-order parameters from bias dependent impedance curves [TvH:6] . Our method consists of measuring, using standard equipment, the electric impedance of aluminum-nitride (AlN) BAW resonators as a function of the frequency for different static electric field. Then, the Mason model [38], based on the first order constitutive equation, is fitted to these characteristics by adjusting the three material parameters of the piezoelectric layer. In contrast to earlier work [39–41], we fitted the impedance not only at the resonance frequency, but also for much lower frequencies. Then the static electric field dependence of the first order piezoelectric parameters is used to calculate the second order piezoelectric parameters.

The bias dependence has been investigated before [42, 43]; however, an explanation for the observed effect was not given. Others discussed the strain dependence of the parameters extensively [44, 45], however, they did not discuss the effect on the impedance curves.

3.3 Resonator Model

In this section we recall the Mason [38] model, which is based on the first order piezoelectric constitutive equations (3.1), for the electric impedance as a function of the frequency, $\omega = 2\pi f$. The electric small-signal impedance Z of the resonator is

$$\begin{aligned} Z =& \frac{1}{j\omega C}\left[1 - K^2 \frac{\tan\phi}{\phi}\frac{(z_r + z_l)\cos^2\phi + j\sin 2\phi}{(z_r + z_l)\cos 2\phi + j(z_r z_l + 1)\sin 2\phi}\right] \\ K =& \frac{e_{33}^2/\kappa_{33}^{\varepsilon} c_{33}^{E}}{1 + e_{33}^2/\kappa_{33}^{\varepsilon} c_{33}^{E}}, \quad \phi = \omega\sqrt{\rho/c_{33}^{D}}\frac{t}{2} \quad c_{33}^{D} = c_{33}^{E} + e_{33}^2/\kappa_{33}^{\varepsilon} \end{aligned} \tag{3.3}$$

where $C = \frac{A\kappa_{33}^{\varepsilon}}{t}$ is the capacitance of the piezoelectric layer, t is the thickness of the piezoelectric layer, A is the area of the device, ρ is the mass density, z_r and z_l are the acoustic impedances of the layers below and on top of the piezoelectric layer. Both are normalized to the acoustic impedance of the piezoelectric layer, given by $\sqrt{c_{33}^{D}\rho}$. K is the piezoelectric coupling coefficient and mainly determines the distance between the resonance valley and anti-resonance peak. The impedance of the layers below the piezoelectric layer is calculated by successive use of the transmission line equation [38]

$$Z_{in} = Z_t \frac{Z_0 \cos\theta + jZ_t \sin\theta}{Z_t \cos\theta + jZ_0 \sin\theta} \tag{3.4}$$

where Z_t is the characteristic impedance of a mechanical transmission line section, given by $Z_t = \rho \cdot v$, Z_{in} is the input impedance of the transmission line, Z_0 is the equivalent terminating impedance attached to the line section and $\theta = \omega t v^{-1}$ is the phase. The last layer of the acoustic mattress is the silicon wafer. To simplify the model an infinitely large substrate thickness is assumed. Here $v = \sqrt{c_{33}^{D}/\rho}$ is the sound velocity.

The static thickness t of the piezoelectric layer for zero external stress, $T_3 = 0$, is approximated by filling in the static parameters in the first order constitutive equation (3.1) by

$$\varepsilon_3 \approx \frac{e_{33}}{c_{33}^E} E_3 \qquad t = t(0)(1+\varepsilon_3) = t(0) + \frac{e_{33}}{c_{33}^E} V \tag{3.5}$$

where V is the bias voltage, and (0) indicates a parameter at zero bias. We will see later that the electric field dependence of t is much smaller than that of the other parameters. From equation (3.5) the mass density dependence on the electric field can be estimated, and hence all input parameters for the Mason model are now available for fitting.

3.4 Devices under Test

In this work we analyse BAW resonators fabricated by NXP Semiconductors. A schematic cross-section of the two resonators characterized in this chapter is shown in figure 3.2 [46]. These resonators are solidly mounted to the substrate. As a result a lot of energy may leak into the substrate. To reduce the corresponding losses an acoustic reflector is mounted between the resonator and the substrate. The AlN film is textured along the crystal [001] axis, this is the piezoelectric active axis. The sample manufacturing is described in [35].

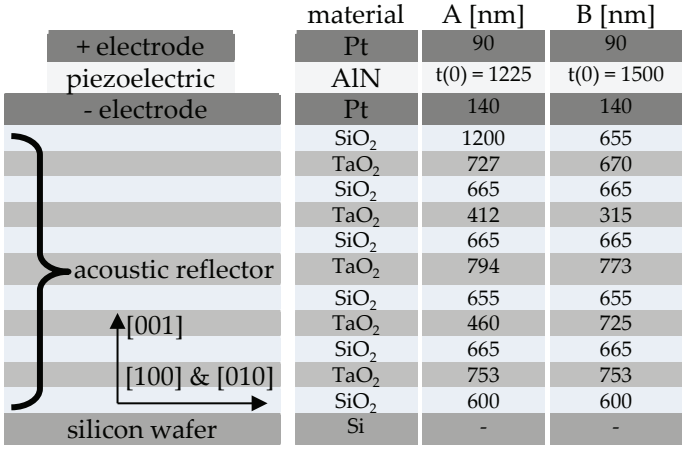


Figure 3.2: Schematic cross-section and dimensions of the BAW resonators. We measured stacks with different layer thicknesses, indicated by resonator A and B. The piezoelectric layer is sandwiched between the metal contacts. The area of the resonator is 182×250 µm.

We measured the electric impedance at room temperature with an Advantest R3767 S-parameter analyser, a schematic of the measurement setup is shown in figure 3.3. A bias voltage, generated by a Keithley K237 supply, is added to the alternating current (AC) signal by a broadband, high

voltage, bias-T [47]. Commercial bias-Tees generally contain a ferroelectric capacitor, which has a strongly bias dependent capacitance. However, this bias-T does not have a ferroelectric capacitor and hence its bias dependence can be neglected.

To compensate for offsets induced by the measurement setup various calibration measurements were performed; short calibration to characterize the connections, open calibration to measure the parasitics; and a 50 Ω test structure to calibrate the high frequency measurements.

We also verified that the high-ohmic silicon substrate did not contribute to the measured static electric field dependence by measuring an open calibration structure containing just the bondpad and connections. In none of the resonators hysteresis was observed.

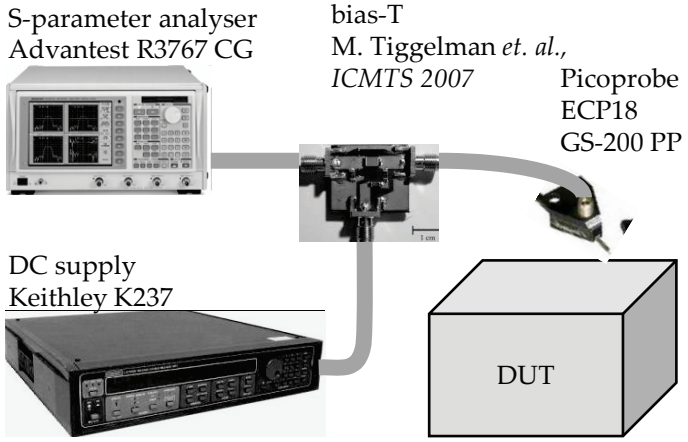


Figure 3.3: Setup used for S-parameter measurements of the resonators.

In figure 3.4 CV and S-parameter recordings are combined to show the impedance over a wide frequency range. We distinguish three frequency regimes. For low frequencies the phase is close to -90 degrees, here the resonator acts as a capacitance. However, around 2 GHz, as shown in the inset, the electro-acoustical coupling results in a resonance valley and anti-resonance peak of the impedance. Altogether there are three frequency regimes, respectively capacitive, resonance and anti-resonance regime. Also there are three unknown coefficients: which are the permittivity $\kappa_{33}^{\varepsilon}$, the stiffness c_{33}^{E}, and the piezoelectric charge constant e_{33}. These can be found by accurate fitting of the model to the electric impedance in the three different frequency regimes.

3.5 Experimental Results

The electrical impedance of the resonators was measured over a large frequency range for various static electric fields. Then, for each static electric field, the Mason model, based on the first order constitutive equation, as

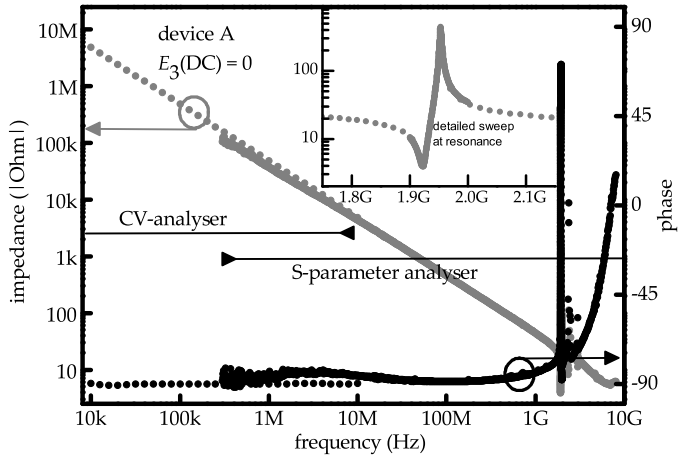


Figure 3.4: Impedance and phase of resonator A, measured with both quasistatic CV meter and S-parameter analyser. The three distinct frequency regimes are recognizable. For a wide part of the range the phase is close to -90 degrees, here the resonator acts as a capacitance. The inset shows a zoom-in of the impedance curve.

shown in section 3.3 was fitted to the measurement data, by minimizing the error of the logarithm of the absolute impedances. With this method the complex impedance was fitted. The fit parameters are the small signal constants of equation (3.1) which now are found as a function of a large static electric field.

Table 3.1: Material parameters as used in the model. ρ denotes the mass density. * marks initial values for the independent fit parameters.

parameter units	ρ [kg/m^3]	c_{33}^E [GPa]	e_{33} [C/m^2]	κ_{33}^ε [$1/\varepsilon_0$]
AlN	3260	370+j·2*	1.4-j0.06*	10*
Pt	21400	373	–	–
SiO2	5728	70	–	–
Ta_2O_5	6970	135	–	–

Table 3.1 lists the used material parameters at zero bias. All parameters are for laterally clamped, thin layers. Both c_{33}^E and e_{33} are complex to account for the small losses in the resonator. The sign of the charge parameter e_{33} depends on the crystal orientation of piezoelectric layer. All coefficients depend on the static electric field E_3 and strain ε_3. In figure 3.5 the capacitances are shown. To obtain an accurate fit a weight factor was introduced for the data below the resonance frequencies. At 0.8 GHz reflector resonances can be observed. The Lakin model contains the reflector and hence these resonances are also present in the modelled data, however, the resolution in the frequency of the measurement data is not

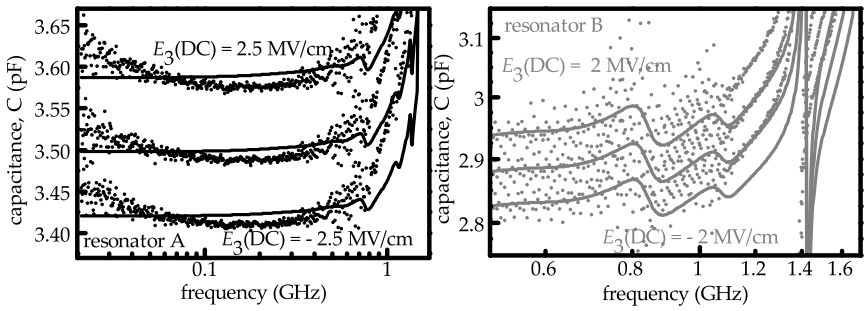


Figure 3.5: The measured (dots) and modelled (lines) capacitance of resonators A and B as function of the frequency. The static electric field was varied, changing the capacitance by thickness and dielectric constant.

high enough to accurately fit the model to the data points in this region. Other secondary effects may arise from substrate resonances and lateral modes and are not captured in the model. However, even without modelling and fitting of these secondary effects an accurate fit can be made.

The static electric field dependence of the capacitance can be explained by both the thickness change of the layer, as in equation (3.5), and the field dependence of the dielectric displacement, as depicted in equation (3.2b). The absolute impedance of the resonators is shown in figure 3.6. Both resonators have a different thickness, resulting in different resonance frequencies and different distance between the resonance and anti-resonance peaks.

The resonance frequencies of the resonators depend on the field bias, as is shown in figure 3.6. This is explained by the change of the piezoelectric layer thickness and by second order parameters of the constitutional equation, as in equation (3.2). Also the distance between the resonance and anti-resonance frequency is field dependent, which is attributed to the change in the coupling coefficient K, and hence of all three first order piezoelectric parameters.

Each data point, plotted as absolute impedance, deviates typically 2% from the model curve, indicating an accurate fit. A part of the error results from the substrate resonances which are not included in the model. We estimate the accuracy of the fitted parameters by adjusting the fit parameters such that the fit error $\sum_f (\log|Z_{meas}| - \log|Z_{model}|)^2$ increases by 10%. The resulting uncertainties are $\pm 0.025\%$ for c_{33}^E, $\pm 0.2\%$ for e_{33}, and $\pm 0.2\%$ for κ_{33}^ε.

3.6 Parameter Extraction

For both resonators the resulting piezoelectric parameters and their static electric field dependence are shown in figure 3.7. The dependence of the

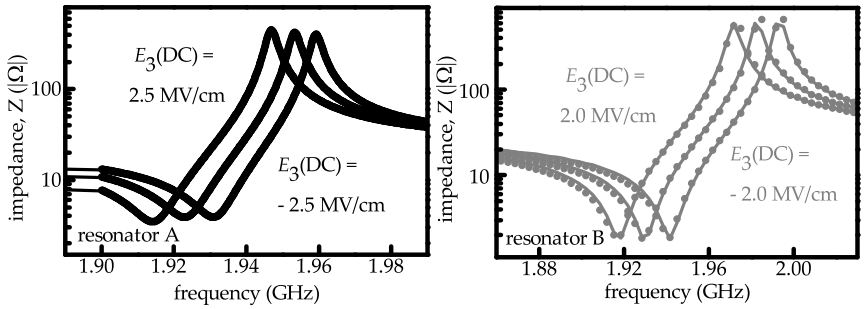


Figure 3.6: The measured (dots) and modelled absolute impedance in the neighbourhood of the resonance frequencies. The electric field was varied, this changes the piezoelectric parameters resulting in a shift of the resonance frequencies. The horizontal distance between the resonance and anti-resonance peak depends on the bias, this results from bias dependence of the piezoelectric coupling coefficient K.

parameters on the bias exceeds the uncertainties of the fitting procedure. No significant electric field dependence of the imaginary part of c_{33}^{E} and e_{33} could be detected. Small differences exist in the extracted parameters for device A and B. We attribute this to inaccuracies of the dimensions and material parameters for layers other than the piezoelectric.

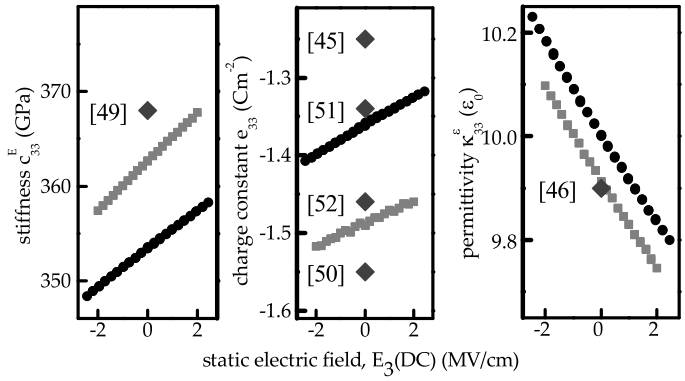


Figure 3.7: The electric field dependence of the piezoelectric parameters, obtained from fitting. From left to right: the stiffness, the charge constant and relative permittivity. The black dots represent data obtained from resonator A, and the grey dots data obtained from resonator B. The black diamonds indicate experimental values obtained from literature [44, 48–52].

The thickness change can be calculated from the piezoelectric parameters and is only +0.04% at 1 MV/cm, while the $\kappa_{33}^{\varepsilon}$ change is about 12 %. Therefore a capacitance voltage measurement [53] [TvH:4] cannot sepa-

rate e_{33} from $\kappa_{33}^{\varepsilon}$ but needs additional information such as the resonance measurement to determine either one of them.

The crystal orientation of the AlN layer and therefore the sign of the electric field cannot be determined by the technique described in this chapter. An independent measurement, for example by wafer bending or optical interferometry would be needed to determine the sign of e_{33}. Here we choose this constant to be negative, which is in line with the expectation that the dielectric constant should drop for positive electric field as in biased electrostrictive materials [45].

The electric field dependence of the fitted first order piezoelectric parameters can be described using the second order piezoelectric equation, see (3.2). Note that the strain is a function of the static electric field in our experiments, see equation (3.5), such that the static electric field dependence of each material parameter is determined by the combination of two δ-parameters. We obtain

$$c_{33}^{E} = \left.\frac{\partial T_3}{\partial \varepsilon_3}\right|_{E_3} \approx \quad c_{33}^{E}(0)\left(1+\delta_3\varepsilon_3-\delta_1\frac{e_{33}(0)}{c_{33}^{E}(0)}E_3\right) \tag{3.6a}$$

$$e_{33} = \left.\frac{\partial D_3}{\partial \varepsilon_3}\right|_{E_3} \approx \quad e_{33}(0)\left(1+\delta_1\varepsilon_3-\delta_2\frac{\kappa_{33}^{\varepsilon}(0)}{e_{33}(0)}E_3\right) \tag{3.6b}$$

$$\kappa_{33}^{\varepsilon} = \left.\frac{\partial D_3}{\partial E_3}\right|_{\varepsilon_3} \approx \quad \kappa_{33}^{\varepsilon}(0)\left(1-\delta_2\varepsilon_3+\delta_4\frac{e_{33}(0)}{c_{33}^{E}(0)}E_3\right) \tag{3.6c}$$

the term (0) has been added to explicitly state that these are the piezoelectric parameters at zero bias, which are equal to the parameters as shown in equation (3.1) and (3.2). Also the six third order coefficients γ_i could be added analogously. There are four second-order terms δ_i and three equations (3.6a-3.6c) to fit to the data shown in figure 3.7. Hence a fourth equation is required. In the next section we will use the non-linear compliance from ultrasound measurements to solve for all δ_i.

3.7 Parameter Comparison

In this section we compare the second order equation for the stress in ultrasound measurements with the second order piezoelectric constitutive equation. If the boundary conditions were equal both equations should be the same. We will show that this holds only if the δ parameters comply with a certain condition. We start with the equations which are generally used in ultrasound measurements [54]

$$D_3 = 0 \tag{3.7a}$$

$$T_3 = c_{33}^{D}(0)\varepsilon_3 + \frac{1}{2}c_{333}^{D}(0)\varepsilon_3^2 + \frac{1}{6}c_{3333}^{D}(0)\varepsilon_3^3 + \ldots \tag{3.7b}$$

where the strain ε_3 is known, and the variables T_3 and D_3 are unknown, however these can be solved from the constitutive equations and equation (3.7a). Once these are found we will compare the result with the constitutive equation for the force, which should be equal. The electric field E_3 is obtained from inserting equation (3.7a) into the constitutive equation for the dielectric displacement D_3. We approximate the electric field with the following series

$$E_3 = \sum_n \frac{1}{n!} a_n (\varepsilon_3)^n = a_0 + a_1\varepsilon_3 + \frac{1}{2}a_2(\varepsilon_3)^2 + \dots$$

and substitute this in the constitutive equation for the dielectric displacement

$$\begin{aligned} D_3 =& e_{33}(0)\varepsilon_3 + \frac{1}{2}\delta_1 e_{33}(0){\varepsilon_3}^2 + \kappa^{\varepsilon}_{33}(0)(1-\delta_2\varepsilon_3)\cdot(a_0 + a_1\varepsilon_3 + \\ & \frac{1}{2}a_2{\varepsilon_3}^2 + \dots) + \frac{1}{2}\delta_4 \frac{\kappa^{\varepsilon}_{33}(0)e_{33}(0)}{c^{E}_{33}(0)}(a_0 + a_1\varepsilon_3 + \frac{1}{2}a_2{\varepsilon_3}^2 + \dots)^2 \end{aligned}$$

and sort this for the powers of ε_3. In the ultrasound measurements no external electric field is applied. Hence when the strain is zero the electric field is also zero. As a result the first order term is zero, $a_0 = 0$, for the displacement we find

$$\begin{aligned} & D_3 = 0 = (e_{33}(0) + \kappa^{\varepsilon}_{33}(0)a_1)\,\varepsilon_3 + \\ & \frac{1}{2}\left(\delta_1 e_{33}(0) + \kappa^{\varepsilon}_{33}(0)a_2 - 2\kappa^{\varepsilon}_{33}(0)\delta_2 a_1 + \delta_4 \frac{\kappa^{\varepsilon}_{33}(0)e_{33}(0)}{c^{E}_{33}(0)} a_1^2\right){\varepsilon_3}^2 + \dots \end{aligned}$$

here the coefficients a_n are readily solved by the condition given in equation (3.7a) that holds for each power of ε_3 individually.

$$a_0 = 0 \quad a_1 = -\frac{e_{33}(0)}{\kappa^{\varepsilon}_{33}(0)}, \quad a_2 = -\frac{e_{33}(0)}{\kappa^{\varepsilon}_{33}(0)}\left(\delta_1 + 2\delta_2 + \delta_4 k^2\right)$$

Hence we have solved the constitutive equation for the dielectric displacement and calculated the electric field as a function of the applied strain. The electromechanical coupling coefficient K and the piezoelectric coupling coefficient k^2 are related by $K^2 = k^2/(1+k^2)$. When we enter the result for the electric field into the constitutive equation for the force, then the result should be the same as equation (3.7b). This yields

$$T_3 = \underbrace{c^{E}_{33}(0)\left(1+k^2\right)}_{c^{D}_{33}(0)}\varepsilon_3 + \frac{1}{2}\underbrace{c^{E}_{33}(0)\left(\delta_3 + k^2\left(3\delta_1 + 3\delta_2 + k^2\delta_4\right)\right)}_{c^{D}_{333}(0)}{\varepsilon_3}^2$$

which can be conveniently written as

$$\frac{c^{D}_{333}}{c^{D}_{33}}\left(1+k^2\right) = \delta_3 + k^2\left(3\delta_1 + 3\delta_2 + k^2\delta_4\right) \tag{3.8}$$

The ratio between the stiffnesses as measured with ultrasound, $\frac{c^{D}_{333}}{c^{D}_{33}}$ is taken from [54]. Although the stiffness in their work is not the same as in ours, we assume that the ratio of the stiffnesses is the same.

Table 3.2: The extracted first and second order piezoelectric parameters. * with a change in sign of e_{33}.

	$c_{33}^{E}(0)$ (GPa)	$e_{33}(0)$ (C/m^2)	$\kappa_{33}^{\varepsilon}(0)$ $(-/\epsilon_0)$	δ_1	δ_2	δ_3	δ_4
A	353	-1.36	10	7.7	-1.6	-7.2	21
B	363	-1.49	9.92	11	-1.4	-7.8	21
A	353	1.36*	10	-20	0.7	-2.5	-20
B	363	1.49*	9.92	-24	0.05	-1.7	-20
[36]				18	0	0	0

3.8 Discussion

We found that the piezoelectric parameters such as the stiffness, charge constant, and permittivity depend on the four δ parameters. However, with equation (3.8) we can eliminate one of the independent parameters. The three independent δ parameters can be extracted from the electric field dependence of the piezoelectric parameters as shown in figure 3.7 and the resultant second order parameters are shown in table 3.2.

We discussed the sign of the piezoelectric charge constant. Hence fitting results with both a negative and a positive charge constant are shown in the table.

Earlier work [36] showed that small resonance frequency shifts are mainly caused by the electric field dependence of the stiffness c_{33}^{E} equation (3.6a). This changes the impedance and results in distortion of the signal. It was shown that the harmonics and intermodulation products could be fitted well using only two parameters, δ_1 and a third-order term γ_4 while setting the other δ to zero. We solved for all four δ parameters, as a result our measured δ_1 minus δ_3 should be comparable with the δ_1 reported earlier, i.e. $\delta_1 - \delta_3$ [this work] = δ_1 [36]. This is the case when a negative piezoelectric charge constant is assumed as was discussed earlier in section 3.6.

The signal distortions caused by the AlN layer also depend on the parametric modulation that is caused by the temperature changes due to the losses within the resonator. A logical next step would be to apply the presented separation technique to measurements at elevated temperatures. Together with thermal modelling [55] this would reduce the number of unknown parameters of a resonator to the non-linearities caused by [001] strain.

For small resonators the clamping condition is not met anymore, therefore lateral acoustic modes can cause parametric modulation. The atomistic origin of the non-linearity of the piezoelectric parameters in AlN thin films is not clear yet. Apart from a bond charge contribution [56] also interfaces and defects like texture, grain boundaries, dislocations or point defects might have an influence.

3.9 Conclusion

In earlier work a single second order parameter of the piezoelectric constitutive relation was measured via distortion measurements. We extracted all four second order parameters from accurate fitting of biased impedance curves using standard measurement equipment. Only one second order property is needed as an external input, which we obtained from ultrasound measurements. Therefore the presented method is an accessible way to find the parameters and to reduce the amount of fit parameters when fitting all nine second and third order parameters. Hence the method addressed in this work opens a path to accurate characterization and modelling of piezoelectric resonators.

In addition this chapter showed that second order parameters derived from the static offset of resonance measurements compare well with literature where the parameters were derived from distortion, which is a measurement of dynamic AC behaviour. Hence we can conclude that the same piezoelectric behaviour is observed for both static DC, and dynamic AC conditions. This also implies that the piezoelectric constitutive equations can be used to predict the performance of the piezoelectric strain modulated FinFET which is introduced in chapter 4.

CHAPTER 4

PIEZOELECTRIC STRAIN MODULATION

In this chapter we study the possibility of piezoelectric strain modulation in a transistor, parts of this chapter have been published [TvH:7] and [TvH:10] .

The goal of piezoelectric strain modulation is to add a novel concept to achieve a steep subthreshold swing. We will propose to compress the fin shaped field effect transistor (FinFET) with a piezoelectric layer to modulate the subthreshold current. The possiblity of current modulation with a piezoelectric layer in an integrated circuit has already been shown [15]. The piezoelectric strain modulated transistor elaborates on this concept, however, we strain each transistor individually, and aim at modulating the subthreshold current using strain.

Recently the piezoelectronic transistor has been proposed [16]. In this device a piezoelectric layer compresses a strongly piezoresistive resistor and thus modulates the resistance. This concept is fairly similar to our piezoelectric strain modulated transistor except for the fact that a very unconventional material is used, instead, we use a standard FinFET.

In chapter 2 the effect of strain on the subthreshold current in narrow FinFETs has been explained. In section 4.1 we recall the relation between strain and subthreshold current, and show that with modulating strain the subthreshold swing can be improved.

In chapter 3 the bias dependence of the strain in a piezoelectric layer was analysed. Section 4.2 shows how the converse piezoelectric effect can induce strain in a semiconducting layer. Four different structures to do so are discussed and the most promising structure is extended to a complete FinFET in section 4.3.

Besides selecting a structure also materials need to be chosen. In section 4.4 the effectiveness of various material combinations for strain mod-

ulation in both an n-type and a p-type FinFET are compared.

In section 4.5 3D strain simulation results are used as an input to a TCAD device simulator. The simulated transfer characteristics of the strain modulated FinFET do show promising results.

The goal of a small subthreshold swing transistor is reduced power consumption. Therefore we discuss the feasibility of strain modulation regarding this goal in section 4.6. Questions regarding the reliability, and performance of the piezo electric strain modulated FinFET are addressed in section 4.7. In the final section 4.8, conclusions are drawn.

4.1 Strain and Subthreshold Current

In this section we investigate the relation between strain and subthreshold current in an n-type FinFET. For a p-type FinFET the theory would be analogous. The subthreshold current can be expressed by an analytical model [4], which in itself is quite extensive. However here we point out only the relevant strain dependent terms. The model is based on Poisson's equation and a solution for the surface potential as a function of the parameter β. The latter is independent of the potential along the channel width, however does depend on the position along the length L, and is solved from the boundary condition

$$\begin{aligned}&\frac{(V_{GS}-\Delta\phi-V_L)}{2u_t}-\ln\left[\frac{2}{w_s}\sqrt{\frac{2\kappa_s\epsilon_0 u_t}{qn_i}}\right]\\&=\ln\beta(L)-\ln[\cos\beta(L)]+\frac{2\kappa_s t_{ox}}{\kappa_{ox}w_s}\beta(L)\tan\beta(L)\end{aligned}\tag{4.1}$$

where q is the elementary charge, u_t is the thermal voltage, $\Delta\phi$ is the gate metal semiconductor work function difference, κ_{ox} and κ_s are the gate dielectric and semiconductor relative permittivity, ϵ_0 is the vacuum permittivity, n_i is the intrinsic carrier density, w_s is the fin width, t_{ox} is the dielectric thickness and V_L is the potential of the channel at a certain point, for example at the drain or source edge.

For narrow FinFETs the channel quantum well in the low-field subthreshold condition results in a constant offset of the band edges; this has no effect on the subthreshold swing and therefore is not taken into account. For a given V_{GS} the parameter $\beta(L)$ can be found from equation (4.1) at both the drain $\beta(D)$ and source $\beta(S)$ side. The drain current is calculated from these variables.

$$\begin{aligned}I_{DS}=&\mu\frac{t_s}{L}\frac{4\kappa_s\epsilon_0}{w_s}(2u_t)^2\\&\cdot\left[\beta\tan\beta-\frac{\beta^2}{2}\frac{\kappa_s t_{ox}}{w_s\kappa_{ox}}\beta^2\tan^2\beta\right]_{\beta(D)}^{\beta(S)}\end{aligned}\tag{4.2}$$

A few percent strain can increase the electron mobility μ in silicon by a factor of three [57–59], while at the same time the subthreshold current may

increase by a factor of 100 [60] due to the band deformation (determined by the bandgap E_G and electron affinity χ_S). Therefore, while invesstigating the effect of the strain on the subthreshold current we can focus on the band deformation solely.

The strain can be taken into account in the model in equation (4.1) via the work function difference $\Delta\phi$ and intrinsic carrier density n_i

$$\begin{aligned} \Delta\phi &= \phi_m - \chi_S - \frac{E_G}{2} \\ n_i &= \sqrt{N_C N_V \exp\left(\frac{-E_G}{u_t}\right)} \end{aligned} \tag{4.3}$$

where ϕ_m is the metal workfunction, N_C the conduction band effective density of states, and N_V the valence band effective densities of states. The electron affinity and band gap are functions of the band edges, this is explained in section B.2. Now we continue with a short summary strain dependence of the band edges.

In silicon the conduction bands become non-degenerate with strain, the so called Δ valleys split up into three different band minima. To simplify matters shear strain is not considered in this section. A model and more elaborate explanation of the band offset can be found in section B.2. Setting the shear strains to zero we find an offset of the three Δ valley pairs

$$E_{\Delta_k}(\varepsilon) = \Xi_d^{\Delta}(\varepsilon_1 + \varepsilon_2 + \varepsilon_3) + \Xi_u^{\Delta}\varepsilon_k \tag{4.4}$$

where Δ_k is one of the three Δ valley pairs corresponding to a large momentum in the k direction, Ξ_d and Ξ_u are the dilatational and uniaxial deformation potential which can be found in table C.8 on page 84, and ε_k is the strain corresponding to direction k, as can be seen in equation (B.3) on page 76. The strain is here explicitly noted in Voigt notation, please refer to section A.1 on page 65 for more details.

The most relevant bands of the valence band are the light hole (LH) and heavy hole (HH) bands; their maxima are located at the Γ point in the reciprocal space. Equation (B.8) on page 78 describes the dependence of the valence band maximum on strain. Setting the shear terms to zero and considering the upper valence band only, then the dependence of the valence band maximum on the strain is given by

$$\begin{aligned} E_{LH}(\varepsilon) = \quad & - \quad a(\varepsilon_1 + \varepsilon_2 + \varepsilon_3) \\ & + \quad \sqrt{\tfrac{b^2}{2}\left((\varepsilon_1-\varepsilon_2)^2+(\varepsilon_2-\varepsilon_3)^2+(\varepsilon_1-\varepsilon_3)^2\right)} \end{aligned} \tag{4.5}$$

where a and b are the deformation potentials, as shown in table C.7 on page 83. As mentioned before both equations (4.4) and (4.5) hold only if the shear strains are zero.

Input parameters for the electical model are the bandgap and electron affinity. In the subthreshold regime the carriers mainly occupy the band

edges and hence the bandgap can be derived from the minimum conduction band and maximum valence band, hence the most negative $E_{\Delta_k}(\varepsilon)$ determines the effective conduction band edge. This is summarized in section B.4.

From equation (4.1) it can be observed that a decrease of the work function difference ($\Delta\phi$) has the same effect on the current as an increase of gate bias (V_{GS}). This can be achieved by a larger electron affinity (χ_S) in equation (4.3), which in turn can be realized with a strong compressive (negative) strain in equation (4.4). In a transistor where the negative strain increases together with the gate source bias (V_{GS}) these two effects would sum up, resulting in an extra increase of the current. To illustrate the effect of strain on the subthreshold current we modelled the current in a silicon FinFET with a V_{GS} dependent strain along the [001] axis (ε_3), the strain along the other axes, (ε_1 and ε_2), is estimated via the ratio of elasticities $-c_{11}/c_{12}$ as shown in table C.4 on page 82.

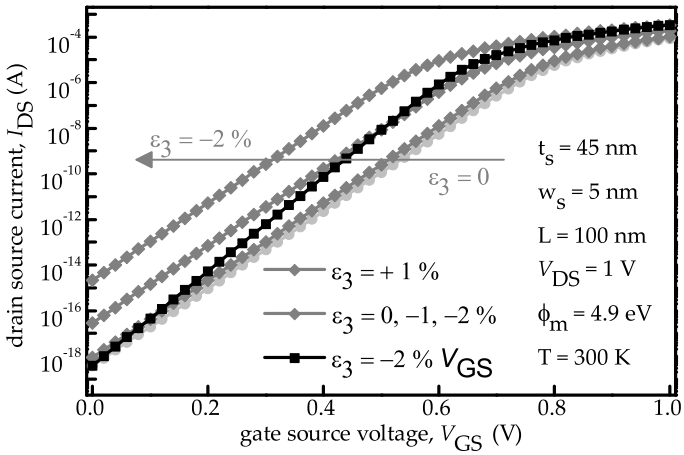


Figure 4.1: Modelled transfer characteristics of a silicon FinFET for static strain and for V_{GS} dependent strain. The V_{GS} dependent strain lowers the conduction band and hence results in an additional increase of the subthreshold current with V_{GS}. As a result the strain modulated device has a steeper subthreshold slope and smaller subthreshold swing. The device parameters are indicated in the figure.

Modelling results according to equations (4.1-4.5) are shown in figure 4.1 for a silicon n-type FinFET. A negative strain results in an exponential increase of the subthreshold current, while a positive strain results in a very small increase. This is due to the negative strain orthogonal to the main strain induced by the Poisson ratio. However, when the strain is dependent on V_{GS} a significant change can be observed. When the transistor turns on, the strain increases, which lowers the conduction band, resulting in an additional increase of the current with the applied V_{GS} and thus a steeper subthreshold slope and smaller subthreshold swing.

4.2 1D Strain Modulation

The previous section showed that a negative strain is required to effectively modulate the subthreshold current in a silicon n-type FinFET. We propose to induce the strain with a piezoelectric material. In piezoelectric materials dipoles are present along one of the crystal axes. If the material is subjected to a mechanical force, these dipoles displace which creates electric charge, this is the piezoelectric effect. The opposite also holds, when subjected to an electric field the material displaces, this is called the converse piezoelectric effect.

It has been shown [15] that a piezoelectric material can be used to strain a substrate through the converse piezoelectric effect and thus modulate the current of transistors on the substrate. However, to reduce the subthreshold swing of a complete integrated circuit, the strain of each transistor has to become a function of its own V_{GS}. To do this effectively a geometry is required which can locally induce a large negative strain into the semiconductor layer.

The relationship between stress and strain is governed by the piezoelectric constitutive equation (A.4) on page 70. In one dimension this is written as

$$T_\pi = -eE + c\varepsilon_\pi, \tag{4.6}$$

where T_π is the stress, e is the piezoelectric charge constant, E the electric field, c the stiffness, and ε_π the strain in the piezoelectric layer. The resultant stress and strain can be maximized by using a piezoelectric material with a large eE product. However, we want to maximize the stress in the adjacent semiconducting layer, therefore the final strain will also depend on the elastic properties and geometries of all other layers besides the piezoelectric layer.

To investigate this relationship we propose four different structures where the application of an electric field oriented along the polar axis of the piezoelectric material induces strain in a semiconducting layer. These structures are a vehicle to explore the most effective way to induce strain, and it may well be impossible to realize the boundary conditions of all four structures in a real device. Therefore the results given in this section represent a best possible estimate of the strain.

The number of different possibilities is reduced by applying forces along the crystal axes only, hence shear strain can be neglected, and by modelling the strain in one dimension only. In these examples Pb(Zr,Ti)O_3 (PZT) is used as a piezoelectric and germanium as a semiconductor material; their properties can be found in table C.4 and C.5 on page 82. The four structures can be differentiated by: the induced strain is either orthogonal or parallel to the applied electric field in the piezoelectric layer, and by: the structure is either free to move or limited on two sides by boundaries. In this chapter the thickness of the piezoelectric is chosen such that the maxi-

mum electric field (E_{cr}) at which the material can still function properly is reached when the supply voltage (V_{DD}) is applied, given by $t_\pi = V_{DD}/E_{cr}$.

4.2.1 Parallel Strain

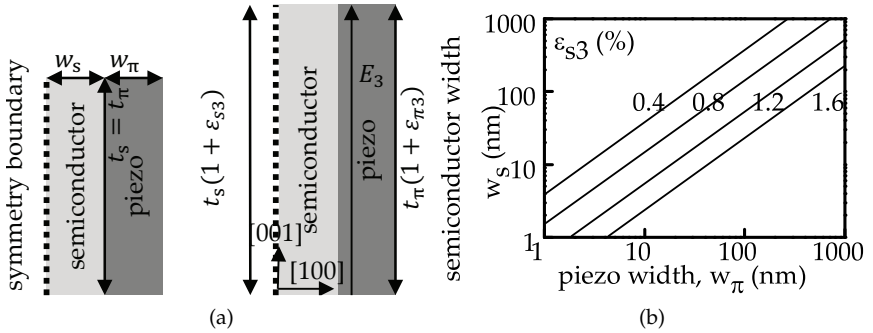


Figure 4.2: (a) Schematic structure where the semiconductor deforms parallel to the applied electric field in the piezoelectric layer. (b) Contour plot of the modelled maximum strain as a function of the width of the layers.

The structure as shown in figure 4.2a contains a piezoelectric layer where the electric field is parallel to the interface with the semiconducting layer. A symmetry boundary condition is applied on the left hand side of the semiconductor, this means that the deformation parallel to the interface can be any, while orthogonal to the interface the displacement has to be zero. This effectively mirrors the structure; without this boundary condition the structure would curve upon application of electric field. Here, and in the rest of the section, the other boundaries are set free to move.

The displacements in the [001] direction in both the semiconductor and the piezoelectric layer have to be equal, hence also the strain values ε_3 in both layers are equal. The layers are modelled as springs with a certain width (w). The force required to induce a certain strain increases with the width. The total force needs to be zero, yielding a boundary condition for the stresses. Hence the following conditions hold

$$\begin{aligned}
&\varepsilon_{s3} = \varepsilon_{\pi 3} \\
&T_{s3} \cdot w_s = -T_{\pi 3} \cdot w_\pi \\
&T_{s3} = \varepsilon_{s3} c_{s33} \\
&T_{\pi 3} = -e_{33} E_3 + c^E_{33} \varepsilon_{\pi 3} \\
&-T_{s3} \tfrac{w_s}{w_\pi} = -e_{33} E_3 + c^E_{33} \varepsilon_{s3}
\end{aligned}$$

from which we derive the strain

$$\varepsilon_{s3} = E_3 \frac{e_{33} w_\pi}{c_{s33} w_s + c^E_{33} w_\pi} \tag{4.7}$$

where the subscripts $_s$ and $_\pi$ differentiate the semiconducting and piezoelectric layer, and the subscript $_3$ denotes the [001] direction. Note that both the piezoelectric charge constant e, and the elasticity for a given electric field c^E, are unique parameters for piezoelectric materials, hence the subscript $_\pi$ has been omitted for these two parameters. Note that in these models the strain is calculated in one direction only, however, the strain in the other directions can be estimated by the ratio $-c_{11}/c_{12}$. This ratio is always smaller than 1, and therefore the strain in the other directions is of less importance.

The dependence of the strain in the semiconductor ε_{s3} on the dimensions is shown in figure 4.2b. For a given piezoelectric layer width the maximum strain can be found by choosing a small enough semiconductor width. This can also be observed in equation (4.7), where for small semiconductor width the grey terms become negligible. Strain values up to 1.7% can be achieved and according to the 1D model the ratio between the widths of the layers determines the final amount of strain.

4.2.2 Orthogonal Strain

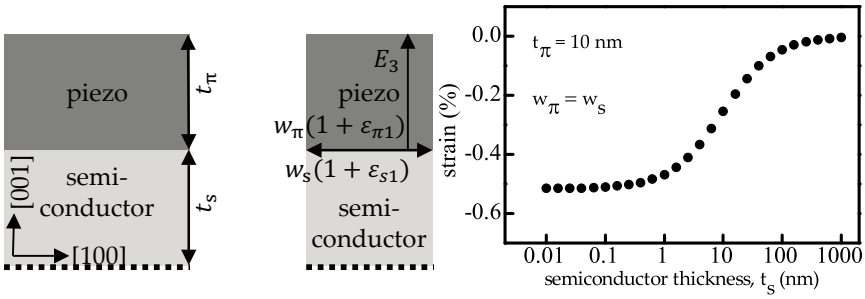


Figure 4.3: (a) Schematic structure where the displacement of the piezoelectric layer orthogonal to the applied electric field is coupled to a semiconducting layer. (b) The induced strain as a function of the semiconductor layer thickness.

Instead of using the deformation parallel to the applied electric field also the deformation of the piezoelectric orthogonal to the electric field can be used to induce strain in the semiconductor layer. An example of such a structure is shown in figure 4.3a. The coupling of the electric field to the stress in the [100] direction is given by: $e_{31}E_3$. The strain ε_1 has to be equal in both layers. The total force should be zero, therefore the sum of the forces multiplied with the corresponding layer width is zero.

Altogether the following boundary conditions hold

$$\begin{aligned}
T_{s1} \cdot t_s &= -T_{\pi 1} \cdot t_\pi \\
\varepsilon_{s1} &= \varepsilon_{\pi 1} \\
T_{s1} &= \varepsilon_{s1} c_{s11} \\
T_{\pi 1} &= -e_{31} E_3 + c_{11}^E \varepsilon_{\pi 1} \\
-T_{s1} \tfrac{t_s}{t_\pi} &= -e_{31} E_3 + c_{11}^E \varepsilon_{s1}
\end{aligned}$$

from this we derive the strain in the semiconductor.

$$\varepsilon_{s1} = E_3 \frac{e_{31} t_\pi}{c_{s11} t_s + c_{11}^E t_\pi} \tag{4.8}$$

The dependence of the induced strain on the thickness of the semiconductor is shown in figure 4.3b. For $t_s < 1$ nm a maximum strain of $\approx$ -0.5% is reached. This can also be seen in the equation for ε_{s1}, see (4.8). For small t_s the grey part in the denominator can be neglected, and hence the strain depends on the properties of the piezoelectric layer only. In other words, the semiconductor layer becomes so small that it can be neglected.

4.2.3 Limited Orthogonal Strain

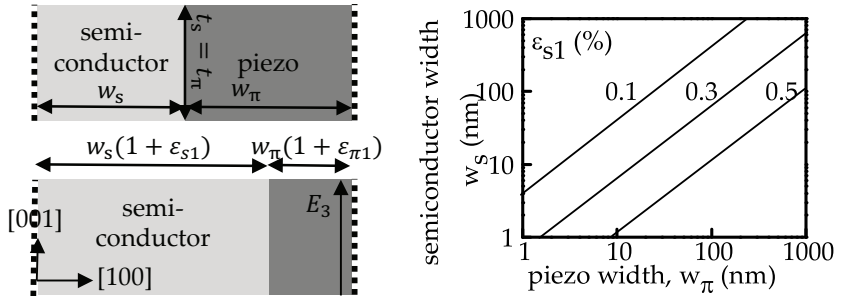


Figure 4.4: (a) Schematic of a structure where the strain induced to the semiconducting layer is orthogonal to the electric field in the piezoelectric layer. The electric field reduces the width of the piezoelectric via the parameter e_{31}. (b) Contour plot of the induced strain dependence on the widths of the layers, the ratio of which determines the strain.

In figure 4.4 a structure is shown, where on both the left and right-hand side symmetry boundaries are applied, i.e. the structure can only move in plane and is confined orthogonal to the symmetry plane. Hence an extension of the piezoelectric material in the direction of the symmetry boundaries results in a compression of the semiconductor layer. Here the stress is constant throughout the structure. The semiconductor is extended by the piezoelectric layer, and hence the stress in the semiconductor is tensile, the semiconductor pulls at the piezoelectric layer, which thus is also

subject to a tensile stress. The sum of the deformations in the [100] direction is zero because the structure is confined to the symmetry boundaries. The following boundary conditions hold

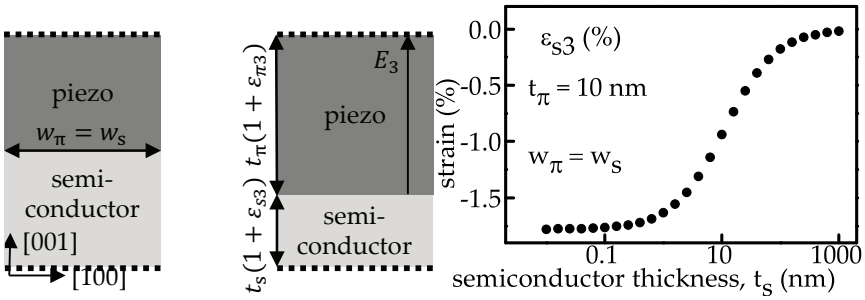
$$\begin{aligned} T_{s1} &= T_{\pi 1} \\ w_s \varepsilon_{s1} + w_\pi \varepsilon_{\pi 1} &= 0 \\ T_{s1} &= c_{s11} \varepsilon_{s1} \\ T_{\pi 1} &= -e_{31} E_3 + c_{11}^E \varepsilon_{\pi 1} \end{aligned}$$

from which the strain can be derived.

$$\varepsilon_{s1} = -E_3 \frac{e_{31} w_\pi}{c_{s11} w_\pi + c_{11}^E w_s} \tag{4.9}$$

When the result is compared with equations (4.8) and (4.7) a minus sign has appeared. This is due to symmetry boundary conditions: an extension of the piezoelectric layers compresses the semiconducting layer. In figure 4.4b the dependence of the semiconductor strain on the widths is shown. A maximum strain is found when the width of the semiconductor is small. This can be observed in equation (4.9), which becomes maximum as soon as the grey coloured term is negligible.

4.2.4 Limited parallel Strain



(a) (b)

Figure 4.5: (a) Schematic structure where the electric field extends the piezoelectric layer in the direction of the field, and due to the symmetry boundaries compresses the semiconducting layer. (b) The dependence of the strain on the semiconductor layer thickness.

Figure 4.5a shows a schematic structure where the electric field extends the piezoelectric layer, which in turn compresses the semiconductor due to the symmetry boundary conditions. In general: $|e_{33}| > |e_{31}|$, see table C.5 on page 82, and therefore this structure is able to induce a large negative strain. The total deformation is zero, and the force is constant throughout the structure. The following boundary conditions hold.

$$
\begin{aligned}
T_{s3} &= T_{\pi 3} \\
t_s \varepsilon_{s3} + t_\pi \varepsilon_{\pi 3} &= 0 \\
T_{s3} &= \varepsilon_{s3} c_{s33} \\
T_{\pi 3} &= -e_{33} E_3 + c_{33}^E \varepsilon_{\pi 3}
\end{aligned}
$$

From which the strain in the semiconductor layer is derived.

$$
\varepsilon_{s3} = -E_3 \frac{e_{33} t_\pi}{c_{s33} t_\pi + c_{33}^E t_s} \tag{4.10}
$$

In this configuration the thickness of the semiconductor can be adjusted to tune the strain. From the model in equation (4.10) it can be observed that for a small semiconductor thickness the grey term becomes negligible and a maximum strain is found. This is also shown in figure 4.5b, where a maximum strain of -1.7% can be found when t_s is in the nanometre range.

4.2.5 Summary

This section discussed four different schematic device structures to induce strain into the semiconductor. Figure 4.1 illustrated that a compressive strain of about -2% would be effective in modulating the subthreshold current. This can be achieved with the structure of subsection 4.2.4, where the largest of the piezoelectric constants, e_{33}, extends the piezoelectric thickness, which due to the symmetry boundary conditions, compresses the semiconducting layer.

4.3 3D Strain Modulation

Section 4.2.4 showed a structure in which a large and compressive strain is induced in the semiconductor layer. However, layers such as the gate, oxide, and contacts to the piezoelectric layers need to be added to obtain a transistor. Therefore we propose the 3D FinFET as illustrated in figure 4.6.

In this structure an extension of the piezoelectric layers along [001] displaces the left and right-hand boundaries. To induce a compressive strain in the fin, symmetry conditions on these boundaries are required; these can be realized by positioning multiple of these strain modulated transistors side by side. Hence the proposed structure is a more sophisticated and rotated version of the structure as shown in figure 4.5. Instead of placing multiple transistors side by side also the placement of solid anchors, on the sides can induce the required boundary conditions.

The axis orthogonal to these boundary planes is the [001] axis, and hence the dipoles in the piezoelectric layer should be oriented along this axis. The electric field in the piezoelectric layer along the [001] axis is given by V_{GS}/w_π.

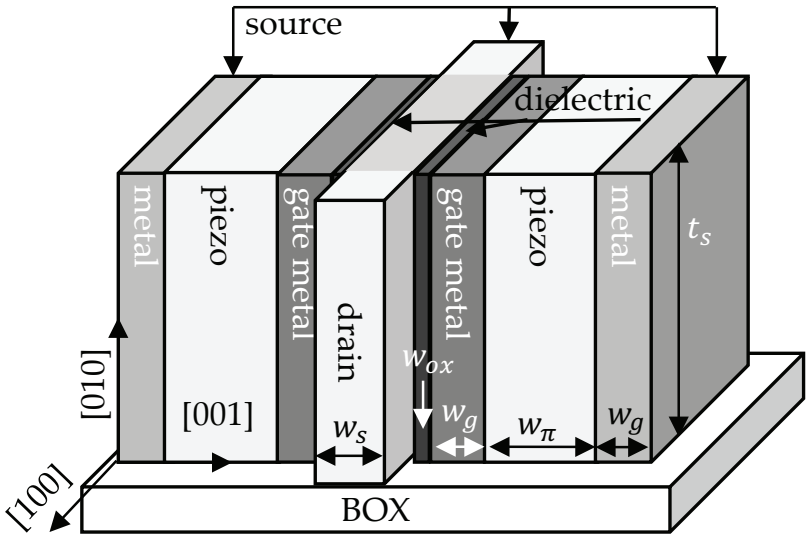


Figure 4.6: The proposed strain modulated FinFET, with gate, oxide, and source layers. The current flow is along the [100]-axis. The extension of the piezoelectric layer along the [001]-axis compresses the semiconductor.

The additional layers may have a significant influence on the net strain in the semiconductor. Hence we continue with the derivation of a 1D model to estimate and understand the parameter and geometry dependence of the strain.

Note that for the gate and dielectric layers an isotropic material model is used, hence $c_{g11} = c_{g33}$ and $c_{ox11} = c_{ox33}$. As the structure is symmetrical we need to model only half of the structure, i.e. from the centre of the semiconducting fin to the metal contacting the piezoelectric layer on either the left or right-hand side. For the sake of convenience the contact to the piezoelectric layer, biased with the source voltage, and the gate are assumed to be of the same material. Again we consider one dimension only. Also the stress (T_3) is equal throughout the layer stack. In 1D the following stress-strain relationships hold.

$$T_3 = \varepsilon_{s3} c_{s33} \qquad T_3 = \varepsilon_{ox3} c_{ox11} \qquad T_3 = \varepsilon_{g3} c_{g11}$$

$$T_3 = -e_{33} E_3 + c_{33}^{E} \varepsilon_{\pi 3}$$

In this structure the total deformation is limited by the symmetry boundary conditions, hence the total deformation is zero.

$$w_s \varepsilon_{s3} + w_{ox} \varepsilon_{ox3} + w_g \varepsilon_{g3} + w_\pi \varepsilon_{\pi 3} = 0$$

We replace the strain terms with their stress equivalents.

$$w_s T_3/c_{s33} + w_{ox} T_3/c_{ox11} + w_g T_3/c_{g11} + w_\pi (T_3 + e_{33} E_3)/c_{33}^E = 0$$

The final stress is found by rearranging terms.

$$T_3 = -\frac{e_{33} V}{c_{33}^E} \left(\frac{w_s}{c_{s33}} + \frac{w_{ox}}{c_{ox11}} + \frac{w_g}{c_{g11}} + \frac{w_\pi}{c_{33}^E} \right)^{-1} \tag{4.11}$$

From this the semiconductor strain cis calculated, given by $\varepsilon_{s3} = T_3/c_{s33}$. The sum of the terms between brackets limits the resulting stress, and hence the individual layer widths may be scaled to tune the strain.

4.4 Material Selection

The most important layers in the structure of the previous section are the piezoelectric and the semiconductor layer. The influence of the oxide can be neglected because it can be very thin, as for the gate metal the selection of a material with a high stiffness maximizes the final strain in the semiconductor. This leaves a piezoelectric layer to be selected which can exert a large force on the semiconductor. This can be evaluated from the stress T_3 in equation (4.11) while minimizing the width of the non-piezoelectric layers.

Secondly a semiconductor needs to be selected which shows a large band deformation per unit applied pressure. To obtain a coarse estimate for the strain we assume that the 1D model holds and that orthogonal strain terms can be neglected, $\varepsilon_{s1} = \varepsilon_{s2} = 0$. The strain in the semiconductor is then given by $\varepsilon_{s3} = T_3/c_{s33}$. The valence band deformation for all the semiconductors shown in this section is given by equation (4.5).

For the conduction band in silicon the minima are at the Δ point with a strain dependence as given in equation (4.4). In germanium the deformation is calculated for the L valleys using equation (B.6). For the III-V materials the valley is at the Γ point and the offset is given by equation (B.7). All the required parameters can be found in tables C.4, C.5, C.7 and C.8 on page 82 to 84.

In figure 4.7 the resulting stress exerted by the piezoelectric layer with a thickness such that $E_3 = E_{cr}$, and V_{DD} = 1 V, is compared with the induced band deformation per applied stress. Contour lines are drawn showing the maximum conduction and valence band deformation for given piezoelectric and semiconductor layer parameters.

For effective strain modulation in an n-type transistor a large conduction band deformation is required, and likewise in a p-type transistor a large valence band deformation is favourable. Figure 4.7 shows that strain modulation, with the structure of section 4.2.4, is most effective in an n-type germanium transistor. Note that if a compound semiconductor (III-V) was chosen a large tensile strain would be required.

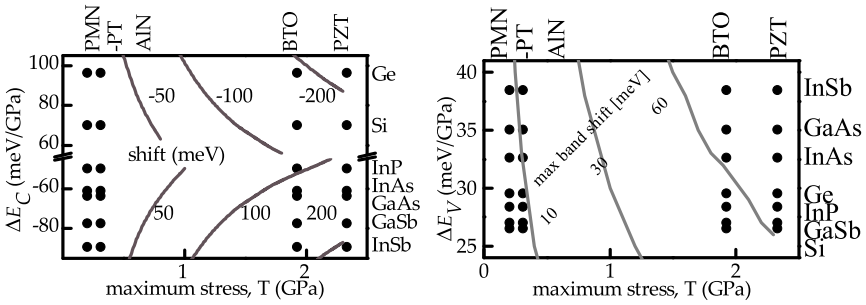


Figure 4.7: The horizontal axis shows the maximum stress $T_{\pi 3}$ by a piezoelectric material, calculated from the piezoelectric parameters and the maximum field according to equation (4.10). On the vertical axis the band edge shift per unit pressure for various semiconductors is shown, according to equations (4.5), (4.4), (B.6) and (B.7). The contour lines show the maximum obtainable band deformation when the structure of section 4.2.4 is assumed. The location of various material combinations on the contour plot is indicated by the dots.

As a piezoelectric material we choose PZT because it can exert the largest stress. PZT is also a ferroelectric material [61], which means that when the electric field changes sign the polarization changes accordingly, yielding negative piezoelectric constants. When the electric field changes sign again the polarization follows accordingly. Therefore we conclude that if the sign of the electric field is constant, then a ferroelectric material can be approximated as a piezoelectric material.

Two layers of piezoelectric material are shown in figure 4.6. When the same V_{GS} bias is applied to these layers, they do have a different direction of the electric field. Furthermore, one of the layers has a negative electric field, therefore, also the dipole orientation will be negative, resulting in an equal $e_{33}E_3$ product [61], and hence the same amount of strain.

A layer of 1.5 nm wide hafnium-oxide (HfO_2) is selected as a gate dielectric because it can be fabricated on germanium and has a relatively high stiffness. For the gate a 5 nm wide titanium-nitride (TiN) is chosen as it is very stiff and has a low resistivity. Additionally a 5 nm wide layer of TiN is used as a source connection. The material parameters for these additional layers can be found in table C.6 on page 83. Note that the model is applied to half of the structure, and hence we choose a 5 nm wide germanium fin, which is taken into the model as 2.5 nm. When we fill in the corresponding numbers in equation (4.11) we find

$$\begin{aligned} T_3 &= \frac{-e_{33}V_{DD}}{c_{33}^E}\left(\frac{w_s}{c_{s33}} + \frac{w_{ox}}{c_{ox11}} + \frac{w_g}{c_{g11}} + \frac{w_\pi}{c_{33}^E}\right)^{-1} \\ &= -1.9\cdot 10^{11}\,(20 + 7.5 + 6.8 + 85)^{-1} = -1.6[\mathrm{GPa}] \end{aligned}$$

where the denominator is determined mainly by the piezoelectric and

the semiconductor layers, as can be observed the numbers, and hence the effect of the gate dielectric and gate metal on the resulting strain is relatively small.

4.5 Simulation Results

In addition to the 1D modelling, 3D FEM simulations [21] have been performed to obtain insight into the resulting strain in the device. A buried oxide (BOX) layer has been added as a substrate, the fin length L is set to 80 nm, and symmetry boundary conditions have been added to the source and drain contacts to mimic the relatively large and stiff metal contacts, and to the metals layers on the left and right hand side which contact the piezoelectric layer.

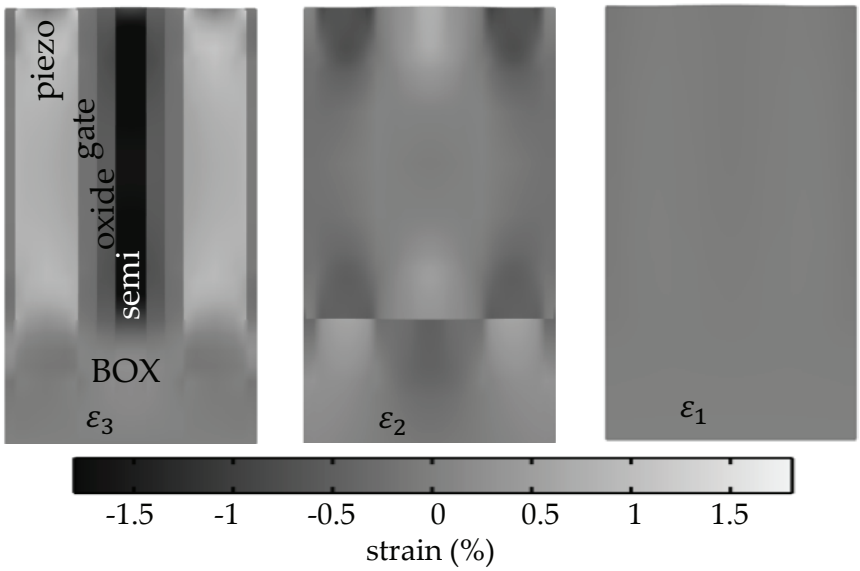


Figure 4.8: Simulated strain on a cross-section along the width, [001] direction, of figure 4.6. Note that the strain is uniform in the semiconducting layer.

In figure 4.8 the simulated strain in the FinFET is shown. Along the width, the [001] axis, the corresponding strain ε_3 is clearly tensile in the piezoelectric layer and compressive in the semiconducting layer. Along the other axes the strain is negligible.

The strong compressive strain, ε_3, can also be observed in figure 4.9, which shows the strain in the length of the device, which is along the [100] axis. From both figures it can be observed that the strain is approximately uniaxial, along one axis: ($\varepsilon_1 = \varepsilon_2 = 0$), and uniformly distributed throughout the fin.

The 1D model gives a value for the strain, while the 3D simulations generate a different strain value for each point in the device. However,

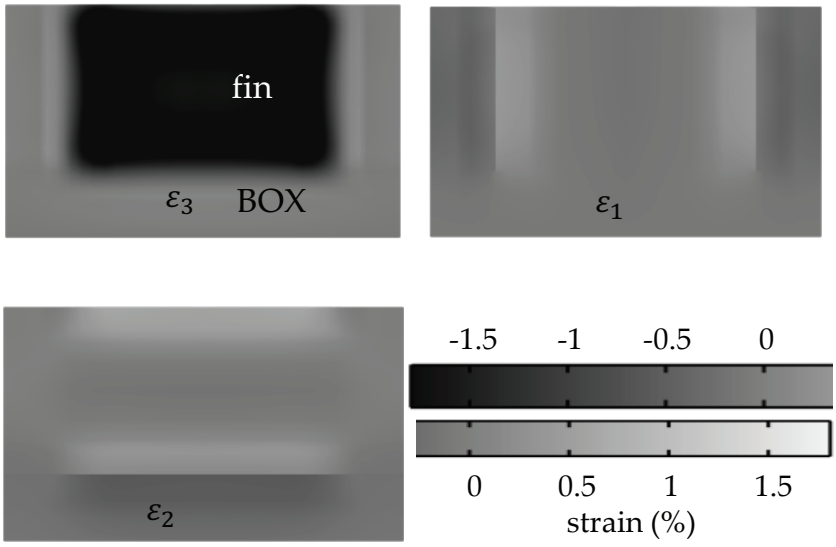


Figure 4.9: Simulated strain on a cross-section along the length of figure 4.6.

figures 4.8 and 4.9 show that the strain is distributed uniformly over the fin volume. Therefore the strain in a given direction can be represented by a single value obtained from averaging the simulated strain throughout the fin volume.

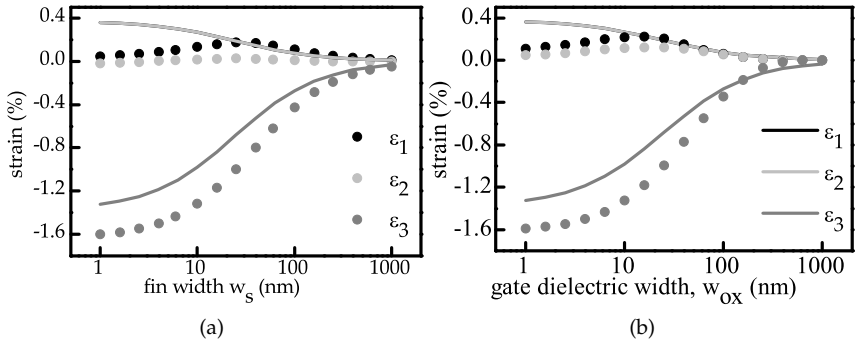


Figure 4.10: Modelled (lines) strain ε_s and simulated (symbols) average strain ε_3 as a function of w_s and w_{ox}, clearly showing an increase for smaller fin width and gate dielectric. The modelled (solid) strain ε_1 & ε_2 are the same.

In figure 4.10 we compare the 1D modelled strain, see equation (4.11), and the averaged simulated strain as a function of both the gate dielectric and semiconductor fin width. Both the 1D model and the 3D simulations show the same qualitative dependence of the strain ε_3 on the dimensions.

The modelled orthogonal strain values ε_1 and ε_2 are estimated from T_{s1}/c_{12}, and increase for small fin width and gate dielectric, while in the simulation they become negligible. Hence we can conclude that for high aspect ratio structures the strain tends to become uniaxial, while for a lower aspect ratio the orthogonal strains ε_1 and ε_2 can be estimated by T_{s1}/c_{12}. A close to maximum strain can be found at a realistic 5 nm fin width.

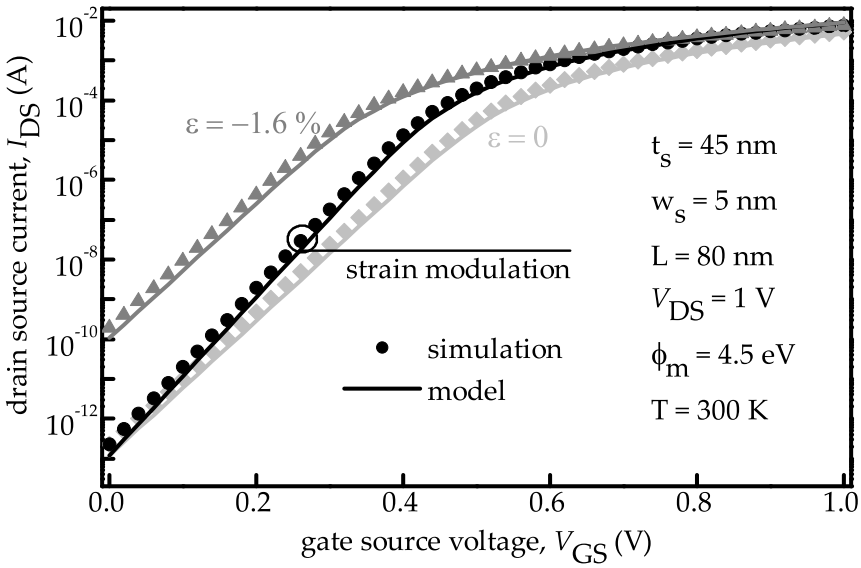


Figure 4.11: Simulated and modelled transfer characteristics of the FinFET illustrated in figure 4.6 with both strain modulation and constant strain. Strain modulation results in a steeper subthreshold slope.

In most semiconductor device simulators the strain is assumed to be a constant, which is not the case with strain modulation. Therefore special care was taken to change both voltage and strain for every bias step. The results of the averaged strains from the FEM simulation are used as an input for the 2D TCAD device simulator [32]. In the proposed strain modulated FinFET the strain is a function of the bias on the piezoelectric layer. This bias depends on the bias of the gate and source contacts only. Hence a self-consistent simulation approach is not required.

From an electrical point of view it does not matter at which height, or position along [010], the structure is simulated, hence it can be simulated in 2D. In the device simulator the strain tensor is a constant throughout the whole fin, as is confirmed by the uniformity of the strain predicted by the FEM simulations, shown in figures 4.8 and 4.9.

Figure 4.11 shows simulated transfer characteristics as well as the result of the analytical current model of section 4.1 for the germanium strain modulated FinFET.

For comparison results for the same devices with constant strain are also shown. The strain modulation combines the off-current of a device without strain with the lower threshold voltage of a device with strain. From the graphs the subthreshold swing is found to be 59 mV/dec for the devices with constant strain, which is the thermal limit for diffusion current. However, with strain modulation the subthreshold swing reduces to 50 mV/dec. Therefore, strain modulation is able to break the thermal limit.

4.6 Power Consumption

The reason to investigate steep subthreshold slope devices is the promise of a lower power consumption. In this section we estimate the effect strain modulation has on the power consumption of a transistor that is used in digital logic circuitry.

The total power consumption can be divided into two parts. The first is the dynamic power P_{dyn}, which in digital logic is the energy required to switch the transistor state [62] and multiplied by the number of switches per second. The second is the static power, given by the leakage current multiplied by the supply voltage.

The strain modulation effect can be used in two different ways. Either the supply voltage V_{DD} is kept the same and the leakage current I_{off} is reduced, resulting in a lower static power, or the I_{off} is kept constant and the supply voltage is reduced, resulting mostly in a lower dynamic power.

In the strain modulated FinFET a piezoelectric capacitance is added parallel to the gate capacitance. For each cycle both must be charged and drained, and as a result this adds up to the dynamic power consumption. Hence it is unlikely that the strain modulated FinFET is able to reduce the dynamic power consumption.

However, it can reduce the leakage power at the cost of an increased dynamic power. We follow [62], and note that the dynamic power (P_{dyn}) is given by the sum of the charge required to charge both the oxide (P_{ox}) and the piezoelectric layer (P_π), and find

$$\begin{aligned} P_{ox} &= WL\alpha f_{clk} f_o V_{DD}^2 0.5 C_{ox} \\ P_\pi &= WL\alpha f_{clk} f_o V_{DD}^2 0.5 \left(\frac{\epsilon_0 \kappa_{33}^{\varepsilon}}{t_\pi} + \varepsilon_\pi e_{33} \right) \\ P_{stat} &= I_{off} V_{DD} \exp\left(\frac{\Xi_{eff} \varepsilon_s}{u_t} \right) \end{aligned} \tag{4.12}$$

where $\alpha = 0.01$ [63] is the switching activity factor, f_{clk} is the clock frequency, C_{ox} is oxide capacitance per unit area, $f_o = 3$ [63] is the tapering factor (the number of switches each transistor has to drive), and I_{off} is the off-current of a device without strain. The band deformation due to the induced strain is given by $\Xi_{eff}\varepsilon_s$, where Ξ_{eff} is the effective deformation

potential. The piezoelectric power scales with the sum of the dielectric constant and the strain in the piezoelectric layer.

The equations can be used to estimate whether strain modulation can reduce the power consumption of a transistor. In the general case we can only answer that it strongly depends on all the material parameters, device dimensions, frequency of operation and usage of the devices. However, we can state that strain modulation can reduce the static power at the cost of an increased dynamic power, hence it can only be beneficial in circuits where the static power dominates the total power consumption.

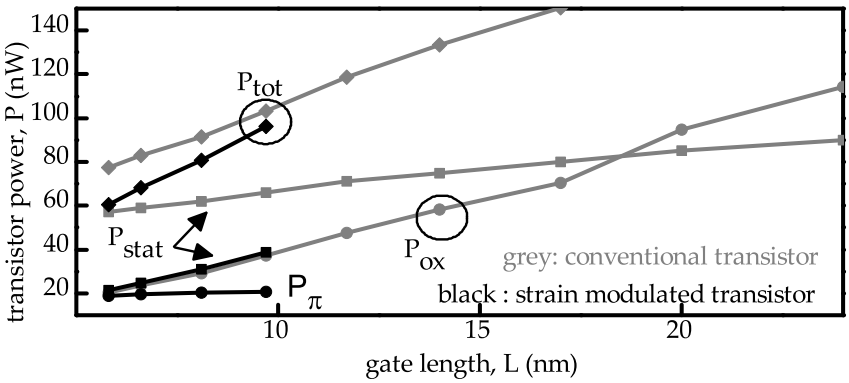


Figure 4.12: In grey the estimated power of an n-type transistor calculated from the ITRS [64] prognoses for device parameters and performance. In black an estimate for the strain modulation effect on the power consumption. Please note that the strain modulation is used to decrease the static power consumption. Hence P_{ox} is the same for both transistors.

An estimation for the device parameters in the future can be found in the ITRS roadmap [64]. From this roadmap we calculated the expected dynamic and static power for an n-type transistor, and these are shown in figure 4.12. The graph shows that the static power consumption exceeds the dynamic power for technologies with gate lengths below 18 nm. Next, we estimated the effect piezoelectric strain modulation can have on the power consumption. We tuned the piezoelectric layer thickness, and thus the strain modulation and corresponding power P_{ox}, to obtain a minimal total power. To illustrate the numbers at L = 5 nm, the tuned piezoelectric thickness is 48 nm, its dielectric constant is assumed to be 150 [ϵ_0], while at this gate length the thickness of the oxide is 0.5 nm.

We found that from 12 nm technologies onward the estimated leakage power is significantly higher than the dynamic power. There the strain modulation can reduce the total power consumption of a transistor, even at the cost of the additional dynamic power consumption of the piezoelectric layer.

4.7 Considerations

In this chapter a linear built-up of the strain even at the critical value of the electric field inside the piezoelectric layer is assumed, this may overestimate the strain, and hence the presented results represent a best-case estimate.

A more straightforward method to induce strain modulation is to replace the gate dielectric in a bulk transistor with a piezoelectric layer. However, the gate source voltage is distributed across the semiconductor and the gate dielectric. For a transistor with an ideal subthreshold swing of 60 mV/dec at room temperature the potential across the dielectric is zero in the subthreshold regime. In this case replacing the dielectric with a piezoelectric layer results in zero strain modulation as there is no potential across the dielectric.

A potential across the dielectric would build up if the subthreshold swing would be higher than the thermal limit. Unfortunately the resulting strain, effect on the band alignment, and hence increase of the subthreshold current, will not be large enough to decrease the subthreshold swing below the thermal limit.

In this work the thickness of the piezoelectric is chosen equal to the fin height. Simulations [16] showed the possibility of increasing the applied stress by increasing the relative volume of the piezoelectric compared to the semiconductor. This solution comes at a significant price. The increase of the piezoelectric volume also increases the dynamic power, and requires additional space on the substrate.

This chapter showed the strain dependence of the FinFET, however, any device with a significant current dependence on the strain is a candidate for strain modulation. An example is the band to band tunneling (B2B) field effect transistor (FET). In figure 4.6 the band diagram of the source-channel junction of the B2B FET is shown. In the on-state the channel potential is raised to such an extent that the valence band has an energy level equal to or even above the conduction band in the source. As a result electrons can tunnel directly from the channel into the source. In the off-state these energy levels do not align resulting in a much lower current. The tunnel current is a function of both the physical distance between the two bands, and the maximum height of the energy barrier separating them [65, 66]. This is illustrated by the triangle in figure 4.13. As an example we sketched also the band diagrams in the presence of strain modulation. We employed the numbers given in figure 4.7 to estimate the bandgap in the on-state. Both the height, which is the given by the bandgap, and the distance of the tunnelling barrier are significantly lowered in the presence of strain. Therefore the B2B FET could be a suitable candidate for strain modulation.

The focus of the chapter was on the strain effect on the subthreshold current. However, for devices also the on-current, and hence the strain

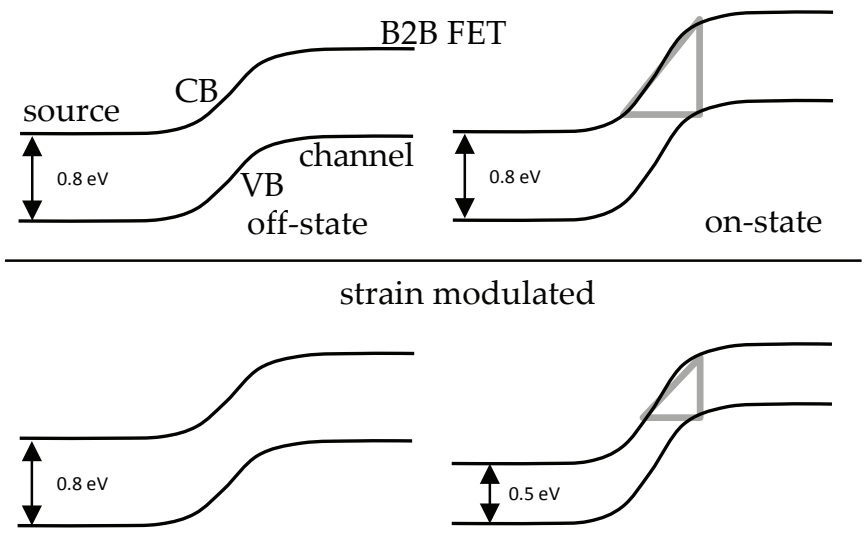


Figure 4.13: Schematic band diagram of a germanium B2B FET. When strain modulation is applied both the tunnelling distance, and barrier, indicated by the grey triangle, are significantly lowered in the on-state.

dependent mobility, needs to be considered. The strain is strongly compressive and orthogonal to the transport direction. In a silicon FinFET this results in an enhanced carrier mobility [17, 24]. In germanium this has a positive effect on the mobility of holes, however, reduces the mobility of electrons slightly [24].

Another issue of concern is reliability, in PZT this is often addressed as fatigue. Fatigue is the reduced polarization of the piezoelectric layer that typically occurs after about 10^9 switches [67], however, in our device the polarization does not switch and hence fatigue may occur after many more switches. Furthermore the presence of lead in the PZT layer which may diffuse into the semiconductor, and the continuous change of the strain inducing delamination could lead to reliability issues.

The speed at which the strain can build up sets a limit to the maximum operating speed of a strain modulated transistor. We estimate this speed with the acoustic velocity, $v_a = \sqrt{c_{33}/\rho}$ where ρ is the mass density [68]. The distance from the edge of the piezoelectric layer to the middle of the fin is about 17 nm. Most of this is in the PZT layer which also has a relatively low acoustic velocity of 2.8 nm/ps. Hence the limit to the operating speed is in the range of 5 ps.

Altogether strain modulation enlarges the input capacitance, this increases the dynamic power consumption. Additionally the use of piezoelectric layer adds limits to both the switching speed and lifetime of a circuit. As a result strain modulation may find applications in low power circuits, or in circuits which do not change state all the time, such as SRAM.

4.8 Conclusions

By combining an analytical current voltage model for a silicon FinFET and a semiconductor band deformation model we showed that a V_{GS} dependent strain can reduce the subthreshold swing.

To induce this strain we propose to use a piezoelectric layer biased with the gate-source voltage V_{GS}. However, the piezoelectric and semiconducting layers need to be combined in an effective way. To do such we compare four different structures. A relatively large strain is required, therefore the most effective structure employs the largest of the piezoelectric coefficients.

To obtain an effective material combination for strain modulation we select a piezoelectric layer that is able to induce a large pressure on the semiconducting layer. The pressure depends on both the piezoelectric charge constant and the maximum field at which the layer still behaves properly. From the studied materials this property is best matched with PZT as a piezoelectric layer. Secondly a semiconducting material is required which shows a large conduction band deformation per applied pressure, for which we select germanium.

Note that if an III-V compound semiconductor was selected a tensile strain would be required to lower the subthreshold swing in an n-type transistor. In this case the structure shown in figure 4.3 would have been selected. For a p-type transistor instead a large valence band deformation per applied pressure, and also compressive strain, would have been required.

We extended the 1D designed structure to a 3D strain modulation germanium n-type FinFET. With finite element method simulation we derived the resulting strain. Both simulation results, and a 1D analytical model, showed that an electric field close to the critical value is favourable to obtain a large strain value. These can be achieved by scaling the thickness such that for a given supply voltage the critical field, the maximum electric field at which the piezoelectric still functions, is reached.

By combining a 3D finite element method and 2D device simulations transfer characteristics of the proposed device were obtained. These showed that with the converse piezoelectric effect the lower off-current of a relaxed transistor can be combined with the lower threshold voltage of a strained transistor. In our example this results in a 50 mV/dec subthreshold swing at room temperature. This is below the theoretical limit of 59 mV/dec for conventional transistors indicating that strain modulation can open a new road to steep subthreshold slope devices.

The additional piezoelectric layer adds a capacitance parallel to the gate capacitance. Thus it increases the dynamic power consumption of a transistor. However, the added negative strain allows having an equal on-state performance, combined with a lower leakage current, for a given supply and threshold voltage. The static power consumption scales with

the leakage current. Hence we can state that the static power has been reduced at the cost of an increase of the dynamic power.

CHAPTER 5

SUMMARY & CONCLUSION

5.1 Strain in FinFETs

We simulated the effect of thermal expansion in narrow fin shaped field effect transistors (FinFETs). The titanium-nitride (TiN) gate metal is deposited at an elevated temperature. When cooled down the TiN gate metal shrinks faster than the silicon fin. This induces a compressive strain in the silicon. The strain is induced in plane with the fin/gate metal interface, therefore a narrower FinFET, which has a smaller volume, and approximately equal size interface, can be expected to have a larger amount of strain. Both finite element method (FEM) simulations and holographic interferometry measurements [17] confirm this.

Compared to the simulations the measurements show a much stronger strain dependence on the fin width. Unfortunately, the measurement results are available for two fin widths only. To obtain a complete strain tensor we fitted the simulation results to the available measurement points.

We described a theory to calculate the band offset in narrow fins due to the sum of both strain and quantum confinement effects.

We also defined a method to demarcate the subthreshold region from measured transfer characteristics. This method is applied to measurements for various temperatures, from which we extract the band offset between a wide and narrow fin. We find that theory and measurement agree.

5.1.1 Conclusions

The strain is induced by the difference in coefficient of thermal expansion (CTE) of the metal gate and the silicon fin, however, the exact amount of strain also depends on the dimensions, elasticities of both materials, and the interfacial layers. This is confirmed by FEM simulation and holo-

graphic interferometry measurements [17], where the strain increases for narrower fins.

Downscaling the fin width has two effects on the band offset: a decrease of the bandgap due to the increase of strain, and for fins narrower than 10 nm an increase of the bandgap due to quantum confinement. This means that, the subthreshold current density increases for fin widths down to 10 nm, and then decreases for even smaller fins.

5.1.2 Recommendations

The strain and quantum confinement effects counteract each other for fin widths near 10 nm. There exists a plateau of the conduction band offset as a function of the fin width. At this plateau the band offset is relatively insensitive to fin width variations. This translates in a lower variation of the leakage current and the threshold voltage.

The exact amount of strain is crucial in this work, an accurate measurement of the strain for various widths and in various dimensions would remove some of the uncertainties in the estimation of strain with simulation results fitted to measurements.

Apart from the effect of the strain on the subthreshold current also its effect on the carrier mobility is relevant. The carrier mobility can be measured by combining capacitance voltage (CV) and transfer characteristics.

5.2 Second Order Piezoelectricity in BAW resonators

In chapter 3 we discuss the frequency response of Bulk Acoustic Wave (BAW) resonators as a function of the static electric field. More specifically, there are three frequency regimes that all show a different dependence on the bias: capacitance, in this regime the impedance is strongly coupled to the permittivity; the resonance frequency, which depends on elasticity; and the anti-resonance frequency, strongly depending on three piezoelectric parameters. The presence of these three distinct frequency regimes and three piezoelectric parameters, allows extracting the piezoelectric parameters independently as a function of the applied static electric field.

The bias dependence of the three piezoelectric parameters can be characterised by four second order piezoelectric parameters. We have shown a theory to reduce the number of independent second order parameters to three by incorporating ultrasonic theory and measurement results. The obtained parameters compare well with published results.

5.2.1 Conclusions

We found that by biasing resonance measurement the second order piezoelectric parameters can be extracted from the data, contrary to the literature where the parameters are estimated from distortion measurements. Hence the proposed method adds an alternative, and simple, method to

extract these parameters. This may contribute to a better prediction of non-linearities. Alternatively, we can conclude that second order parameters derived from the static offset of resonance measurements compare well with literature where the parameters were derived from distortion, which is a measurement of alternating current (AC) behaviour. Hence we can conclude that the same piezoelectric parameters apply for both static DC, and dynamic AC conditions.

5.2.2 Recommendations

The proposed method lacks the ability to determine the sign of the piezoelectric charge constants e_{33}. The addition of laser vibrometer measurements could remove this uncertainty.

In this thesis we have shown that the proposed method works in these specific BAW resonators. The method relies on an accurate measurement of the complex impedance across an extended frequency range. This may be not possible at all if the material shows a significant leakage current.

The measured static electric field dependence of the piezoelectric parameters appear to be linear, however, a small non-linearity is present to which the third order parameters could be fitted. Therefore our proposed method may be extended to extract the first, second and third order parameters.

Also BAW resonators show some small signal loss, which means that they dissipate power, and hence they are likely to heat up during operation. Therefore a prediction of the behaviour of BAW resonators is not complete without knowledge of the temperature dependence of the parameters.

5.3 Piezoelectric Strain Modulation

In chapter 4 we focus on a concept to reduce the subthreshold swing of transistors. This number determines the required threshold voltage for a given leakage current. A relatively low subthreshold swing can be achieved with the FinFET or Tri-Gate transistor. Compared with a conventional MOSFET the FinFET has an improved electrostatic control over the channel because the gate surrounds it. However, the subthreshold swing is still limited by the thermal limit for diffusion transport of 60 mV/dec at room temperature. To obtain a transistor with an even lower subthreshold swing an alternative device concept is required.

In this work, we combine a model for the subthreshold current and band offset as a function of the mechanical strain. It is found that the subthreshold current scales exponentially with negative (compressive) strain. This also means that when the strain is dependent on the applied gate voltage, the induced band offset can contribute to a smaller subthreshold swing.

We propose to induce this voltage dependent strain with a piezoelectric layer. We find that the most effective structure for a strain modulated transistor employs a piezoelectric material that has a large product of dielectric strength and piezoelectric charge constant.

This concept is used in the strain modulated FinFET, which is a FinFET with a piezoelectric layer at the sidewalls. To obtain maximum strain in the semiconducting fin we propose to place a multiple of these devices side by side. This effectively results in symmetrical boundary conditions.

By combining 3D FEM and 2D TCAD simulations we obtain transfer characteristics for a strain modulated transistor. These show a 9 mV/dec lower subthreshold swing than the thermal limit of 60 mV/dec at room temperature of diffusion transistors.

5.3.1 Conclusions

We have shown that a voltage dependent strain can reduce the subthreshold swing of conventional transistors. To obtain effective strain modulation a structure is required in which a large compressive stress is applied to the semiconductor layer. This is realized by selecting a piezoelectric material that has a large piezoelectric coefficient multiplied with the dielectric strength. The semiconductor layer itself should have a large band deformation per applied pressure.

The design of an effective device structure for strain modulation depends on the type of semiconductor. Both indirect band gap semiconductors silicon and germanium require a negative strain, while the compound semiconductor (III-V) require a positive strain to increase the subthreshold current in an n-type transistor.

A positive piezoelectric strain can induce negative strain (or vice versa) in the semiconductor by applying stiff or symmetry boundaries to sandwich the piezoelectric and semiconducting layer.

We have shown that a lower subthreshold swing can be achieved by strain modulation. However, this is not necessarily saving power. The addition of a piezoelectric capacitance increases the dynamic power consumption of a strain modulated integrated circuit. Hence the strain modulation concept is able to reduce the leakage current at the cost of an increase in the dynamic power. In other words, if the static power is the dominant power in an integrated circuit, then the static power can be reduced by strain modulation at the cost of a larger dynamic power.

5.3.2 Recommendation

The physics of strain modulation apply to any device where the relevant characteristics are strongly dependent on strain. For example the bipolar junction transistor (BJT), metal oxide semiconductor field effect transistor (MOSFET), or simple diode could also be strain modulated to improve the characteristics. The piezoelectric layers, which are required to induce the

strain, need to be oriented such that an effective strain is induced into the semiconductor, while at same time the contacts to the piezoelectric layer should form neither an electrical, nor a mechanical barrier to the proper functioning of the device.

In this work the application of axial strain on the band offset is investigated, however, the shear strain could be used instead. An advantage could be the strong dependence of the effective masses, and hence the mobility, on the shear strain. This could be of particular interest for a device that aims at strain modulation in the strong inversion regime. Here both a lower threshold voltage and higher mobility as function of the gate source voltage contribute to a larger signal amplification.

This would be of particular interest for an acoustic resonator transistor. In such a device the piezoelectric layer is designed such that it resonates when the wavelength of the acoustic wave matches with the transistor dimensions, this results in particularly high strain values.

To obtain a larger amount of strain in the semiconductor a piezoelectric layer with a larger surface area [16] than the fin may be used. In our design this corresponds to a piezoelectric layer that is higher and longer than the FinFET itself.

5.4 Original Contributions

- We showed that in FEM simulations the strain in narrow FinFET depends on the fin width, as was shown earlier in measurements [17].
- We showed that for very narrow FinFETs, where the strain increases for smaller fins, the band gap narrows due to strain and from 10 nm fin width and below widens due to quantum confinement.
- We developed an alternative method and theory to derive the second order piezoelectric parameters from static biased measurements in, and just below, the resonance regime of aluminum-nitride (AlN) BAW resonators.
- We showed how a material combination can be chosen such that a large strain can be induced in a semiconductor by a piezoelectric layer.
- We simulated and modelled the piezoelectric strain modulated FinFET, a device concept which can achieve sub 60 mV/dec subthreshold swing in a diffusion-based transistor at room temperature. However ,we have also shown that this not necessarily results in a reduced power consumption of an integrated circuit.

APPENDIX A

STRESS IN CRYSTALS

According to Newtons second law of motion a rigid body is accelerated when a force is applied. The body is assumed to be rigid, which implies that the external force is transmitted immediately the whole body. Neither the internal structure of the body, nor the bonding forces which hold the body together are considered. However, in this section the effect of the external forces on the forces inside the non-rigid body, called stresses, and deformations, called strain, is studied.

Stress in a material does not cause strain (nor does strain cause stress), but the two are coupled to each other [69]. The presence of either necessarily implies that the other is also present. Figure A.1 illustrates the effect of longitudinal and shear stress on the shape of a cubic structure. Note that for pure shear strain the volume of the unit cell is not changed.

When discussing the type of strain induced by external forces to a body generally the type of stress, tensile or compressive, and the number of axes along which the stress is applied, are specified. For example when a thin layer of silicon is grown on a germanium substrate, the larger lattice constant of germanium compared to silicon results in to stress. In plane the lattice of the silicon is extended and hence there is a tensile stress along two of the axes. Out of plane there is no stress, hence the stress is biaxial tensile. The resultant strain in the silicon is in plane tensile, and out of plane compressive. The result is an in plane tensile strain in the silicon, and a compressive out-of-plane strain as the material tends to minimize the volume change.

A.1 Stress and Strain

We assume a linear relation between stress and strain and hence we follow Hooke's law

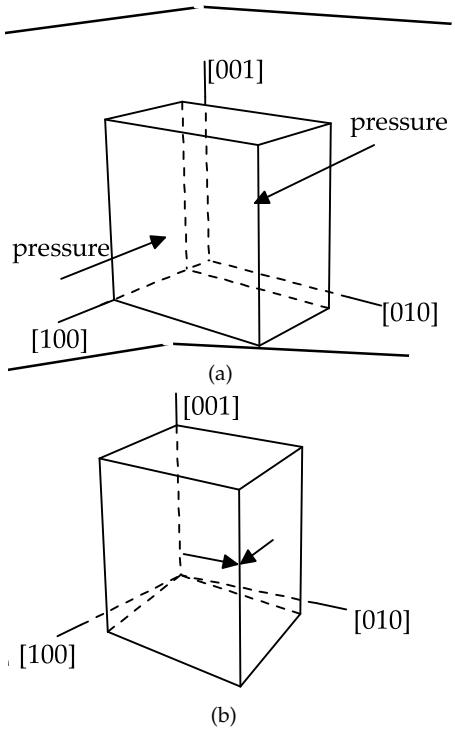


Figure A.1: (a) Negative stress $T_1 = T_{xx}$ in a cubic structure results in a compression along [100]. (b) a shear stress $T_6 = T_{xy}$ tends to extend the cube in the direction $[110] = xy$.

$$T = c\varepsilon$$

here the strain ε is dimensionless and hence the elasticity c has units of stress. Both stress and strain are a single numbers in one dimension. However, in three dimensions the stress must be written as a matrix

$$T = \begin{bmatrix} T_{xx} & T_{xy} & T_{xz} \\ T_{yx} & T_{yy} & T_{yz} \\ T_{zx} & T_{zy} & T_{zz} \end{bmatrix}$$

here the subscripts x, y, z indicate matrix notation [69]. The stress components on the diagonal are the longitudinal stresses, while the other components represent shear stresses. The body must be in both lateral and rotational equilibrium, hence we find

$$T_{xy} = T_{yx}, \quad T_{yz} = T_{zy}, \quad T_{zx} = T_{zx}$$

this reduces the number of independent stress components to six. Both stress and strain can be expressed as 6 x 1 column vectors [68], this is called the Voigt notation. We denote the matrix notation with the subscripts x, y and z and the Voigt notation with subscripts 1 - 6. Note that x and 1

represent a quantity along the [100] axis, y and 2 along the [010] axis and z and 3 along [001].

$$\varepsilon = \begin{bmatrix} \varepsilon_1 \\ \varepsilon_2 \\ \varepsilon_3 \\ \varepsilon_4 \\ \varepsilon_5 \\ \varepsilon_6 \end{bmatrix} \qquad T = \begin{bmatrix} T_1 \\ T_2 \\ T_3 \\ T_4 \\ T_5 \\ T_6 \end{bmatrix}$$

The longitudinal stress matrix components are equal to their Voigt equivalents. However, the relation between the strain in matrix and Voigt notation is given by [69].

$$\varepsilon_4 = 2\varepsilon_{yz} = 2\varepsilon_{zy} \quad \varepsilon_5 = 2\varepsilon_{xz} = 2\varepsilon_{zx} \quad \varepsilon_6 = 2\varepsilon_{xy} = 2\varepsilon_{yx}$$

Hooke's law in three dimensions can also be written conform the Voigt notation, which is given by

$$\begin{bmatrix} T_1 \\ T_2 \\ T_3 \\ T_4 \\ T_5 \\ T_6 \end{bmatrix} = \left[\begin{array}{ccc|ccc} c_{11} & c_{12} & c_{13} & c_{14} & c_{15} & c_{16} \\ c_{21} & c_{22} & c_{23} & c_{24} & c_{25} & c_{26} \\ c_{31} & c_{32} & c_{33} & c_{34} & c_{35} & c_{36} \\ \hline c_{41} & c_{42} & c_{43} & c_{44} & c_{45} & c_{46} \\ c_{51} & c_{52} & c_{53} & c_{54} & c_{55} & c_{56} \\ c_{61} & c_{62} & c_{63} & c_{64} & c_{65} & c_{66} \end{array}\right] \begin{bmatrix} \varepsilon_1 \\ \varepsilon_2 \\ \varepsilon_3 \\ \varepsilon_4 \\ \varepsilon_5 \\ \varepsilon_6 \end{bmatrix} \tag{A.1}$$

where the elasticity matrix can be separated in four regions. The upper left region couples the longitudinal stresses and strains, and is relevant for all materials. The diagonal terms in this region couple stresses and strains in the same direction. The off-diagonal terms couple stress and strain in orthogonal directions. The lower right region couples shear stresses and strains. The diagonal terms are always present, the non-diagonal terms may or may not appear depending on the properties of the material. The lower left and upper right regions couple shear stress with longitudinal strain and vice versa, and may be non-zero depending on the internal structure of the material.

A.2 Elasticity Matrices

The actual elasticity matrices may contain much fewer terms compared to the one shown in equation A.1. This depends on the internal structure of

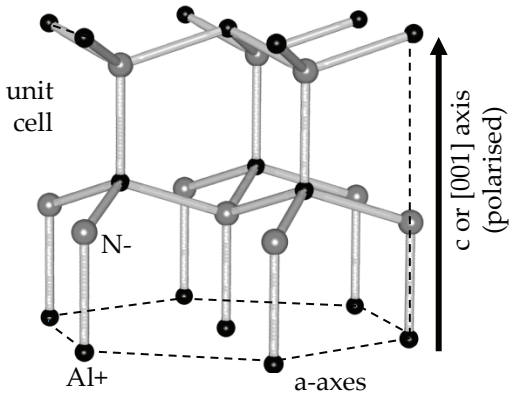


Figure A.2: The unit cell crystal structure of AlN. [70]

a material. In this thesis the non-piezoelectric materials are modelled as isotropic materials, with the following elasticity matrix

$$c = \begin{bmatrix} c_{11} & c_{12} & c_{12} & 0 & 0 & 0 \\ & c_{11} & c_{12} & 0 & 0 & 0 \\ & & c_{11} & 0 & 0 & 0 \\ & & & c_{44} & 0 & 0 \\ & & & & c_{44} & 0 \\ & & & & & c_{44} \end{bmatrix} \tag{A.2}$$

where the not shown numbers in the half below the diagonal are symmetric to numbers above the diagonal. For example $c_{61} = c_{16}$. These materials have an equal stiffness in all directions. The component c_{44} can be written as a function of c_{11} and c_{22}. For semiconductors an anisotropic material with a cubic symmetry is assumed, which results in the same components as the isotropic elasticity matrix, however, with an independent c_{44}.

A.3 Polar Crystals

The piezoelectric materials in this thesis have an asymmetrical structure along one of the crystal axes. In figure A.2 the crystal structure of AlN is shown, a commonly used material with an asymmetrical structure along one of the axes. A hexagonal symmetry can be observed. In the a-plane an atom is surrounded by six other atoms at equal distance. Strain along the c-axis displaces the charge asymmetrically and hence polarizes the material. As a result piezoelectric materials become polarized when subject to a force. This effect is called piezoelectricity, which means "pressing" electricity [68], and forms the link between electrical and mechanical phenomena in a material. It was discovered by J. Curie and P. Curie in 1880 as

the ability of certain crystalline materials to develop an electric charge proportional to an applied mechanical stress. Soon afterwards it was realized that piezoelectricity has to be converse, a geometric strain results from an applied voltage. In non-piezoelectric materials stress automatically implies the presence of strain, in piezoelectric materials however, both are also coupled to the polarization and vice versa.

All materials polarize to some degree, an electric field causes a physical separation between positive and negative charge, creating a dipole moment and hence electric displacement. In piezoelectric materials the polarization can also be created by a strain or stress, which deforms the crystal lattice and causes charge separation. The resultant dielectric displacement is the sum of the displacement due to the electric field and the strain. The total stress is given by the sum of the stress due to strain, and the stress to deformation of the crystal caused by the electric field, which results in the piezoelectric constitutive equations, in one dimension given by

$$D = \kappa^{\varepsilon} E + e\varepsilon \tag{A.3a}$$

$$T = -eE + c^{E}\varepsilon \tag{A.3b}$$

where D is the displacement, κ^{ε} is the dielectric permittivity, e is the piezoelectric charge constant and ε is the strain. The superscript ε denotes that permittivity is measured for a constant strain, and E that the elasticity is measured at a constant electric field. For example, when an electric field is applied both displacement and strain are produced, the strain in its turn couples to a stress that changes the relation between displacement and electric field. In three dimensions the material may have different structures along the various axis. In this thesis the piezoeelectric materials have a hexagonal structure. This implies that the material can be rotated along the c-axis, which is generally chosen as the [001]-axis in the coordinate system, implying that the coefficients for the [100] and [010] axes strain should be equal. Using further hexagonal symmetry rules the

following three dimensional constitutive relations can be found

$$\begin{bmatrix} T_1 \\ T_2 \\ T_3 \\ T_4 \\ T_5 \\ T_6 \end{bmatrix} = \begin{bmatrix} c_{11} & c_{12} & c_{13} & 0 & 0 & 0 \\ & c_{11} & c_{13} & 0 & 0 & 0 \\ & & c_{33} & 0 & 0 & 0 \\ & & & c_{44} & 0 & 0 \\ & & & & c_{44} & 0 \\ & & & & & c_{66} \end{bmatrix} \begin{bmatrix} \varepsilon_1 \\ \varepsilon_2 \\ \varepsilon_3 \\ \varepsilon_4 \\ \varepsilon_5 \\ \varepsilon_6 \end{bmatrix} - \begin{bmatrix} 0 & 0 & e_{31} \\ 0 & 0 & e_{31} \\ 0 & 0 & e_{33} \\ 0 & e_{15} & 0 \\ 0 & e_{15} & 0 \\ 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} E_1 \\ E_2 \\ E_3 \end{bmatrix} \tag{A.4a}$$

$$\begin{bmatrix} D_1 \\ D_2 \\ D_3 \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 & e_{15} & 0 \\ 0 & 0 & 0 & e_{15} & 0 & 0 \\ e_{31} & e_{31} & e_{33} & 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} \varepsilon_1 \\ \varepsilon_2 \\ \varepsilon_3 \\ \varepsilon_4 \\ \varepsilon_5 \\ \varepsilon_6 \end{bmatrix} + \begin{bmatrix} k_{11} & 0 & 0 \\ 0 & k_{11} & 0 \\ 0 & 0 & k_{33} \end{bmatrix} \begin{bmatrix} E_1 \\ E_2 \\ E_3 \end{bmatrix} \tag{A.4b}$$

The polarity required for piezoelectric response can also be formed in an isotropic polycrystalline medium, by temporary application of a strong electric field. This process called poling is analogous to the magnetizing of a permanent magnet. This is explained by the presence of small spontaneously polarized regions in the material, which all become polarized in the same direction due to the strong applied electric field.

There are also some materials in which the spontaneous electric polarization of the crystal can be changed by an external electric field. These materials are called ferroelectric and a typical example is $Pb(Zr,Ti)O_3$ (PZT). This is a perovskite material that shows a rather large piezoelectric effect. The material has 8 lead (Pb) atoms occupying the corners of the unit cell, see also figure A.3.

The crystal structure is shown in figure A.3, and is a so called perovskite. The faces of the unit cell are occupied by Oxygen (O) atoms. The centre of the unit cell is occupied by either a zirconium (Zr) or a titanium (Ti) atom.

In a PZT both centre atoms are present and the ratio between Zr and Ti that allows tuning of the crystallographic phase and hence material properties. In bulk, the largest piezoelectric coefficients are found when the ratio is Zr ≈ 0.53, Ti ≈ 0.47, which is the morphotropic phase boundary, where the material is in between the tetragonal and rhombohedral phase [71]. The names of the phases are derived from the shape of the unit cell.

The central atom of the unit cell, either Zr or Ti, is spontaneously displaced, this is called polarization. The application of a strong electric field can reverse the position of the Zr or Ti atom. An example of PZT is shown in figure A.3. If the field would have been applied in the opposite direction the central atom would have displaced downwards, resulting in an

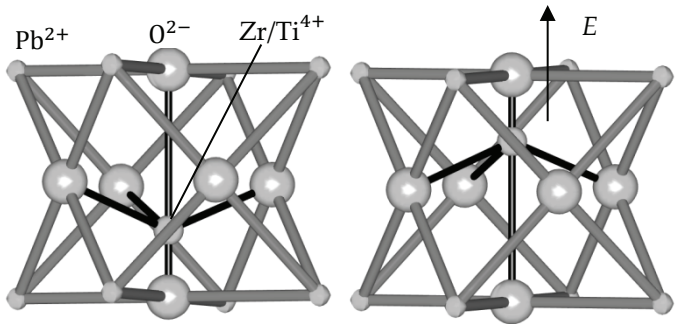


Figure A.3: The unit cell of PZT. The material is polarized which can be changed by the application of electric field. As the dipole orientation can be reversed the material is also ferroelectric.

opposite charge of the dipole. As a result the polarization depends on conditions applied in the past. This is called hysteresis and makes the material not only piezoelectric, but also ferro-electric (FE).

APPENDIX B

STRAIN AND BAND OFFSET

In this chapter the relation between strain and the band structure of various semiconductors is investigated. In the first section we employ silicon as an example to discuss the semiconductor band structure dependence on strain. Then formulas are given to relate the strain to the resultant deformation of the conduction band minima and valence band maxima.

B.1 Lattice Calculations

The size of the silicon unit cell as shown in figure B.1 is given by the lattice constant a_0 and is about ≈ 0.5 nm Hence a wafer, or even a narrow fin as discussed in section 2.1 is much larger than a single unit cell and the semiconducting layer in a transistor can be approximated by an almost infinite number of repetitions of the unit cell. These repetitive boundary

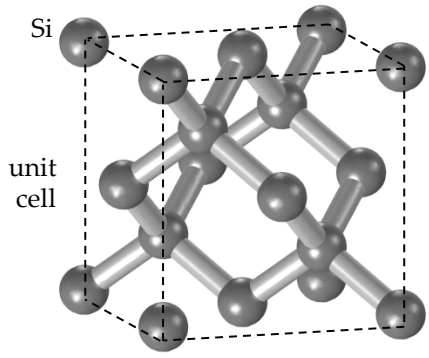


Figure B.1: The unit cell crystal structure of Silicon

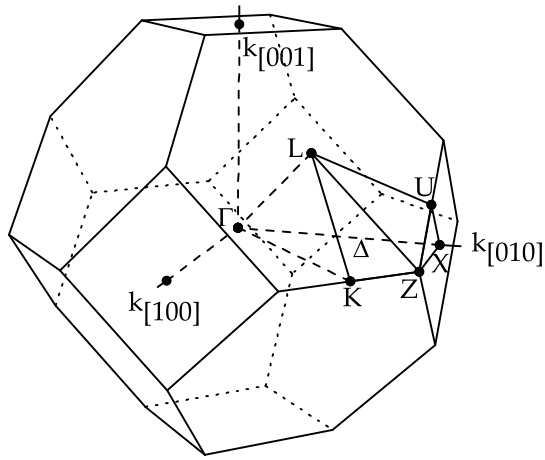


Figure B.2: Illustration of the first Brillouin zone in the reciprocal space. Due to symmetry conditions the band structure needs to be calculated only in the irreducible wedge. The Δ bands are located between Γ = $(0, 0, 0)$ and X = (±1,0,0),(0,±1,0), (0,0,±1) points in units of $[\frac{2\pi}{a_0}]$.

conditions can be applied to Schrödinger's equation and the energy levels available to electrons can be found.

However, the result does depend on the momentum of the electron. Or to state this differently, the available energy levels to electrons depend on the speed at and the direction in which the electron travels. Hence the Schrödinger equation needs to be solved for every possible momentum in the momentum (reciprocal) space, which is shown in figure B.2.

The lattice repetitiveness holds also in the reciprocal space. As a result any point outside the first Brillouin zone has an equal point inside the Brillouin zone, therefore it is necessary to calculate the solutions for the Schrödinger equation inside the first Brillouin zone only. With further symmetry operations it can be shown that the band structure needs to be calculated for the so called irreducible wedge only. The minimum of the conduction band in silicon is found at ≈ 85% of the line between the Γ and any of the six X points in the reciprocal space. These are called the Δ bands, when discussing the minima we call these minima the Δ valleys.

When strain is present in a material the unit cell deforms accordingly. This also induces a change in the reciprocal space, causing it to lose some of the symmetries. It can be shown that the resultant conduction band minima in silicon are still in the Δ bands between the Γ and X points in the reciprocal space. However, the strain reduces the degeneracy and hence every of the Δ valley pairs has a different energy level.

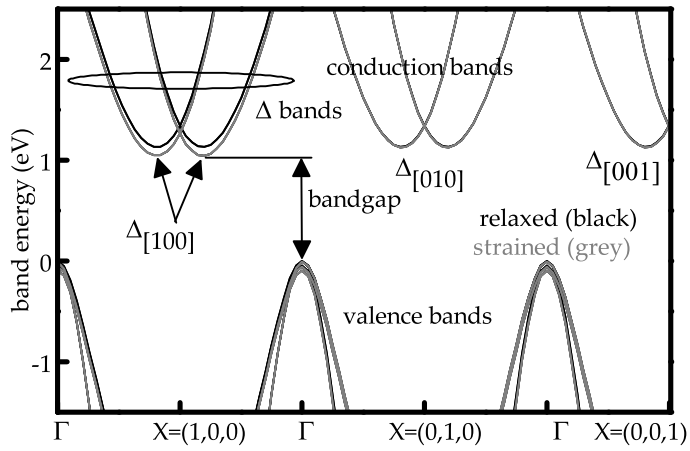


Figure B.3: The band structure of silicon between the Γ and various X points. With 1% uniaxial strain the bands deform.

B.2 Conduction Bands

B.2.1 Silicon

As an example we now investigate the conduction band minimum in silicon when a uniaxial compressive strain is applied. We obtain the band energy levels from a sp3d5s model simulator [72]. In figure B.3 the resulting available energy levels for various parts of the Brillioun zone are shown. The bands are shown for a relaxed and for an uniaxial strained silicon. The graph illustrates that each of the Δ valleys displaces differently due to the applied strain.

Close to the band minima the shape of the band, as a function of the momentum k, can be approximated as an ellipsoid. The dispersion relation couples the energy above of a band minima ν, for example $\Delta_{[100]}$, to the momentum [26]

$$E(k) = E_0 + \frac{\hbar^2}{2}\left[\frac{(k_{[100]} - k_{\nu,[100]})^2}{m_{[100]}} + \frac{(k_{[010]} - k_{\nu,[010]})^2}{m_{[010]}} + \frac{(k_{[001]} - k_{\nu,[001]})^2}{m_{[001]}}\right] \tag{B.1}$$

where $\hbar$ is the reduced Plank constant, while the effective masses are defined as

$$\frac{1}{m_k} = \frac{1}{\hbar^2}\left(\frac{\partial^2 E(k_\nu)}{\partial k_k^2}\right) \tag{B.2}$$

where m is the effective mass, and can be derived along for any momentum k.

In figure B.3 it can be observed that a strain of 1 % changes the positions of the valleys slightly. As long as the strain values are reasonably small the effect on the shape of the valleys is small. Therefore the result-

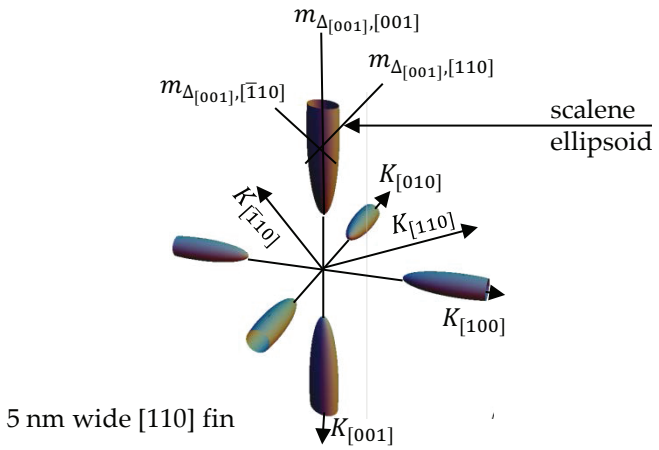


Figure B.4: Illustration of the equi-energy surfaces of the silicon Δ band minima in the presence shear strain ε_6 and compressive strain ε_3. The effective masses to describe the dimensions of scalene ellipsoids of the [001] valleys are shown.

ing change of the energy levels can be written as a linear function of the strain [14, 23]

$$\begin{aligned} E_{\Delta_{[100]},\varepsilon} &= \Xi_d(\varepsilon_1+\varepsilon_2+\varepsilon_3)+\Xi_u\varepsilon_1 \\ &+ \begin{cases} -\frac{\Theta}{4\kappa^2}\varepsilon_4^2 & |\varepsilon_4|<\kappa \\ -(2|\frac{\varepsilon_4}{\kappa}|-1)\Theta/4 & |\varepsilon_4|\geqslant\kappa \end{cases} \end{aligned} \tag{B.3a}$$

$$\begin{aligned} E_{\Delta_{[010]},\varepsilon} &= \Xi_d(\varepsilon_1+\varepsilon_2+\varepsilon_3)+\Xi_u\varepsilon_2 \\ &+ \begin{cases} -\frac{\Theta}{4\kappa^2}\varepsilon_5^2 & |\varepsilon_5|<\kappa \\ -(2|\frac{\varepsilon_5}{\kappa}|-1)\Theta/4 & |\varepsilon_5|\geqslant\kappa \end{cases} \end{aligned} \tag{B.3b}$$

$$\begin{aligned} E_{\Delta_{[001]},\varepsilon} &= \Xi_d(\varepsilon_1+\varepsilon_2+\varepsilon_3)+\Xi_u\varepsilon_3 \\ &+ \begin{cases} -\frac{\Theta}{4\kappa^2}\varepsilon_6^2 & |\varepsilon_6|<\kappa \\ -(2|\frac{\varepsilon_6}{\kappa}|-1)\Theta/4 & |\varepsilon_6|\geqslant\kappa \end{cases} \end{aligned} \tag{B.3c}$$

where Ξ_d, Ξ_u and the dilatational and uniaxial deformation potentials for a given conduction band zone, Θ is the band separation between the two lowest conduction bands at the conduction band edge of the unstrained lattice [14]. The dimensionless parameter $\kappa = \Theta/(4\Xi_{u'})$ depends on the deformation potential responsible for the band splitting of the two lowest conduction bands at a given zone, which in the silicon case is given by the Δ valley [14].

The energy levels of the band valleys depends on the strain, however, also the shape of the bands changes. The effective masses are dependent on the shape, and therefore they are strain dependent. In this thesis the only non-zero shear strain component is ε_6, which does not affect the effective masses of the $\Delta_{[100]}$ and $\Delta_{[010]}$ valleys [14, 26], however it does affect

the $\Delta_{[001]}$ valleys. The shear strain ε_6 removes some of the crystal symmetries, the ellipsoids that describe the shape of the bands close to their minima become scalene (have a different length along each axis). This is illustrated in figure B.4. The shape of the scalene ellipsoids of the $\Delta_{[001]}$ bands can be described by three effective masses in the [001], [110] and $[\bar{1}10]$ directions

$$m_{\Delta_{[001]},[001]} = \begin{cases} m_l(1-\varepsilon_6^2/\kappa^2)^{-1} & |\varepsilon_6| < \kappa \\ m_l(1-\kappa/|\varepsilon_6|)^{-1} & |\varepsilon_6| > \kappa \end{cases} \tag{B.4a}$$

$$m_{\Delta_{[001]},[110]} = \begin{cases} m_t(1-\eta\varepsilon_6/\kappa)^{-1} & |\varepsilon_6| < \kappa \\ m_t(1-\mathrm{sgn}(|\varepsilon_6|)\eta)^{-1} & |\varepsilon_6| > \kappa \end{cases} \tag{B.4b}$$

$$m_{\Delta_{[001]},[\bar{1}10]} = \begin{cases} m_t(1+\eta\varepsilon_6/\kappa)^{-1} & |\varepsilon_6| < \kappa \\ m_t(1+\mathrm{sgn}(|\varepsilon_6|)\eta)^{-1} & |\varepsilon_6| > \kappa \end{cases} \tag{B.4c}$$

where η is a unit less parameter, and m_l m_t are the longitudinal and transversal electron masses of the Δ band minima in relaxed silicon.

B.2.2 Germanium

In germanium the conduction band offset can be calculated likewise as in silicon, however, the minimum is not at the Δ point as in silicon, but at the L point in the reciprocal space. The offset of valley i in the reciprocal space is given by [73]

$$E_C^i = (\Xi_d \bar{1} + \Xi_u \{\hat{a}_i \hat{a}_i\})\varepsilon \tag{B.5}$$

where Ξ_u and Ξ_d are the uniaxial and dilation deformation potentials, $\bar{1}$ is the unit matrix, $\{\}$ note the dyadic product from Balslev [74], $\{\hat{a}_i \hat{a}_i\} = \sum_i \sum_j a_{ij} b_{ij}$, and ε is the strain matrix. If the shear strain terms are zero we find and equal deformation for each of the eight L valleys.

$$E_L(\varepsilon) = (\varepsilon_1 + \varepsilon_2 + \varepsilon_3)\left(\Xi_u^L + \Xi_u^L\right) \tag{B.6}$$

B.2.3 Compound (III-V) materials

For the compound materials used in this work the conduction band minimum is at the Γ point. The offset due to strain is given by [73].

$$E_\Gamma(\varepsilon) = a_c\,(\varepsilon_1 + \varepsilon_2 + \varepsilon_3) \tag{B.7}$$

B.3 Valence Bands

The valence bands of all the selected semiconductors in this thesis have maxima at the Γ point. In this thesis the subthreshold regime is investigated, here the number of carriers is low and holes reside only in the upper valence band (VB), hence the third hole band with a maximum close to

the Γ point, the split off band, which is 44 meV (silicon), or 296 meV (germanium) below, can be neglected. The dependence of the valence bands on the applied is strain is given by [23, 32, 73, 75]

$$\begin{aligned} E_{LH}(\varepsilon) &= -a(\varepsilon_1+\varepsilon_2+\varepsilon_3) \\ &+ \sqrt{\tfrac{b^2}{2}\left((\varepsilon_1-\varepsilon_2)^2+(\varepsilon_2-\varepsilon_3)^2+(\varepsilon_1-\varepsilon_3)^2\right)+d^2(\varepsilon_4^2+\varepsilon_5^2+\varepsilon_6^2)} \end{aligned} \tag{B.8a}$$

$$\begin{aligned} E_{HH}(\varepsilon) &= -a(\varepsilon_1+\varepsilon_2+\varepsilon_3) \\ &- \sqrt{\tfrac{b^2}{2}\left((\varepsilon_1-\varepsilon_2)^2+(\varepsilon_2-\varepsilon_3)^2+(\varepsilon_1-\varepsilon_3)^2\right)+d^2(\varepsilon_4^2+\varepsilon_5^2+\varepsilon_6^2)} \end{aligned} \tag{B.8b}$$

where, a, b and d are the deformation potentials.

B.4 Bandgap and Electron Affinity

If the carrier density is low then only the minimum of the conduction band valleys and maximum VB valley are occupied. As an example we show the effective electron affinity and bandgap for silicon

$$\chi_S = \chi_{S0} - \min(E_{\Delta_k}) \tag{B.9a}$$

$$E_G = E_{G0} + \min(E_{\Delta_k}) - \max(E_{HH}, E_{LH}) \tag{B.9b}$$

where E_{G0} and χ_{S0} is the relaxed bandgap and electron affinity respectively.

APPENDIX C

PARAMETERS

Table C.1: List of Physical Constants

Boltzmann's consant	k_B	$8.61738 \cdot 10^{-5}$ eV/K
electron rest mass	m_0	$9.1\ 10^{-31}$ kg
elementary charge	q	$1.60218 \cdot 10^{-19}$ C
electron Volt	eV	1 eV = q J
vacuum permittivity	ϵ_0	$8.85418 \cdot 10^{-14}$ F/cm
Planck's constant	h	$6.62617 \cdot 10^{-34}$Js
reduced Planck's constant	$\hbar$	$= \frac{h}{2\pi} = 1.05458 \cdot 10^{-34}$ Js

Table C.2: List of Symbols

A	area
a_0	lattice constant
a_c	conduction band deformation potential at the Γ point
a	valence band deformation potential
b	valence band shear deformation potential
c	elasticity
d	valence band shear deformation potential
e	piezoelectrical charge constant
D	dielectrical displacement
E	electric field
E_{cr}	critical electric field
$E_{\Delta_k}(\varepsilon)$	Δ valley offset as a function of the strain
$E_k(n)$	valley offset due to quantum confinement
$E_{\Delta_k}(\varepsilon, n)$	total Δ valley offset ($= E_{\Delta_k}(\varepsilon) + E_k(n)$)
$E_{LH}(\varepsilon)$	offset of the light hole band as a function of the strain
$E_{HH}(\varepsilon)$	offset of the heavy hole band as a function of the strain
E_G	bandgap
E_{G0}	relaxed (ε=0) bandgap
I_{DS}	drain-soure current
k_w	wavenumber in the direction of the channel width
k	momentum in reciprocal space
K	piezoelectric coupling coefficient
κ_{ox}	permittivity of the oxide
κ_s	permittivity of the semiconductor
L	channel length
L	points in reciprocal space located at $k = [\pm\frac{1}{2},\pm\frac{1}{2},\pm\frac{1}{2}]$
m_l	longitudinal effective mass ($\varepsilon = 0$)
m_t	transversal effective mass ($\varepsilon = 0$)
$m_{\nu,k}$	electron effective mass of valley ν in the direction k
N	number of parallel fin shaped field effect transistors (FinFETs)
N_C	conduction band effective density of states
n_i	instrinsic carrier density
N_V	valence band effective density of states
ν	acoustic velocity
V_{DD}	supply voltage
V_{DS}	drain-source bias
V_{GS}	gate-source bias
V_T	threshold voltage
V_L	potential at certain point (L) in the channel
w	position along the channel width
w_g	width of the gate metal
w_{ox}	width of the dielectric
w_s	width of the semiconductor layer
w_π	width of the piezoelectric layer

T	stress
t_{ox}	oxide layer thickness
t_{π}	piezoelectric layer thickness
u_t	thermal voltage k_BT/q
z_r	relative acoustic impedance of layers below piezoelectric layer
z_l	relative acoustic impedance of layers above piezoelectric layer
X	points in reciprocal space located at [±1,0,0] and [0,±1,0] and [0,0,±1]
Z_t	characteristic impedance of transmission line section
Z_{in}	transmission line impedance
Z_0	equivalent terminating impedance

Table C.3: List of Greek Symbols

$\beta(S)$	β solved at the source side
$\beta(D)$	β solved at the drain side
Γ	point in reciprocal space located at k = [0,0,0]
δ_i	second order piezoelectric parameters
$\Delta\phi$	semiconductor metal work function difference
Δ	valley between the Γ and X point in the reciprocal space
ε	strain
ε_1	strain along the [100] axis
ε_2	strain along the [010] axis
ε_3	strain along the [001] axis
ε_4	shear strain in the [100] plane
ε_5	shear strain in the [010] plane
ε_6	shear strain in the [001] plane
η	dimensionless parameter
Θ	deformation model paramater
κ	dimensionsless deformation parameter
μ	carrier mobility
Ξ_d	dilatational deformation potential
Ξ_u	uniaxial deformation potential
$\Xi_{u'}$	deformation potential for splitting of the two lowest conduction bands (CBs)
ρ	mass density
ϕ_m	metal work function
χ_S	semiconductor electron affinity
χ_{S0}	relaxed (ε=0) electron affinity
Ψ	electron wave function
ω	frequency in radians

Table C.4: Elasticity parameters for semiconductors.
The notation of elasticity in [76] is unclear, compared to literature [73, 77] a factor 10 error seems to be present.

	a_0 (0.1 nm)	c_{11}	c_{12} (GPa)	c_{44}	
Si	5.431	165.77	63.93	76.92	[24, 77]
	5.43	167.5	65.0	79.6	[14]
	5.43	167.5	65.0	80.1	[73]
Ge	5.658	128.53	48.26	66.80	[24, 77]
	5.65	131.5	49.4	68.4	[73]
GaAs	5.653	112.6	57.1	60.0	[77]
	5.65	122.3	57.1	60.0	[73]
	5.63	122.1	56.6	60.0	[76]
GaSb	6.096	88.34	40.23	43.22	[77]
	6.08	90.8	41.3	44.5	[73]
	6.1355	87.69	43.41	40.76	[76]
InAs	6.058	82.29	45.26	39.59	[77]
	6.0583	83.29	45.26	39.59	[76]
	6.08	83.3	45.3	39.6	[73]
InSb	6.479	69.18	37.88	31.32	[77]
	6.48	65.9	35.6	30.0	[73]
	6.4794	68.47	37.35	31.11	[76]
InP	5.869	101.1	56.1	45.6	[77]
	5.87	102.2	57.6	46.0	[73]
	5.8697	101.1	56.1	45.6	[76]

Table C.5: Elasticity and dielectric parameters for piezoelectric materials.
[a] the dielectric constant κ is estimated for large fields

	c_{11}^E (GPa)	c_{33}^E	e_{33} (C/m^2)	e_{31}	E_{cr} (MV/m)	κ_{33}^ε (ϵ_0)	ρ (kg/m^3)	
AlN	345	395	1.55	-0.48	200	9.5		[49]
	402.5	387	1.34	-0.6		9.5	3260	[50]
	396	373						[78]
					≈500	9.9		[52]
					400-1200	4-11		[79]
			1.29	-0.38				[44]
BTO	150	146	17.5	-4.35	110[80]	2000[80]	5700	[68]
PMN-PT	115	103	20	-3.9	10[81]	680	8060	[82]
PZT	127	117	23	-6.6	100[83]	150[a] [83]	7500[68]	[84]

Table C.6: Elastic parameters for various materials.
[85] the data was interpolated from comparable compounds.
[86] the ρ calculated and measured for $HfSiO_4$.
[87] the CTE was measured for $HfSiO_4$.
[a] as used in chapter 3.
[b] from private communication with NXP Semiconductors.
[c] to our knowledge not available.

	c_{11} (GPa)	c_{12} (GPa)	ρ (kg/m^3)	CTE (10^{-6}/K)	ε_{lim} (%)	k (ϵ_0)
Si	See C.4			3.5 [88]	3 [89]	
Ge	See C.4					15.8
poly-Si	160[88]	35 [90]		6.4 [88]	2 [90]	
SiO_2	57[91] 70[a,b]	11.4 [91]	5728[a,b]	0.6 [92]	2 [93]	
HfSiO	110 [85]	0.2[86]		3.6 [87]	[c]	
HfO_2	220[94]	66[95]				22[32]
TiN	640 [96]	160 [96]		9.4 [22]	5 [97]	
Pt	373[b]		21400[b]			
Ta_2O_5	135[b]		6970[b]			

Table C.7: Deformation potentials at the Γ point.
[73] data is given as : theory, experimental.
[76] uses a different sign convention for a_c.

	a_c	a	b	d	E_G (eV)	
Si		2.1	-2.33	-4.75		[24]
		-2.3	-5.5	1.16		[77]
	1.98	2.46	-2.35,-2.1	-5.32,-4.8	1.17	[73]
Ge		2.0	-2.16	-6.06		[24]
	-1.8	-7	-1.8	-7.0	0.794	[77]
	-8.24	1.24	-2.55,-2.9	-5.5,-5.3	0.74	[73]
GaAs			-2.79	-7.5	1.518	[77]
	-7.17	1.16	-1.9,-1.7	-4.23,-4.5	1.518	[73]
	-7.17	1.16	-2.0	-4.8	1.519	[76]
GaSb			-1.6	-5.0	0.812	[77]
	-6.85	0.79	-,-2	-,-4.8	0.75	[73]
	-4.5	1.4	-1.35	-4.3	0.812	[76]
InAs			-1.72	-3.3	0.416	[77]
	-5.08	1.00	-1.55,-1.8	-3.10,-3.6	0.41	[73]
	-5.08	1.00	-1.8	-3.6	0.417	[76]
InSb			-2.3	-5.2	0.234	[77]
	-6.17	0.36	-,-2.1	-,-5.0	0.24	[73]
	-6.94	0.36	-2.0	-4.7	0.235	[76]
InP			-1.6	-4.2	1.425	[77]
	-5.04	1.27	-,-1.6	-,-4.2	1.42	[73]
	-6	0.6	-2.0	-5.0	1.4236	[76]

Table C.8: Deformation Potentials for the Δ and L valley.
[a] Ξ_d are calculated from $\Xi_d + \Xi_u/3 - a$, with a taken from [24].

	Ξ_u^Δ	Ξ_d^Δ	Ξ_u^L	Ξ_d^L	$\Xi_{u'}$	Θ	κ	η	
	(eV)						(-)		
Si	9.29	1.1			7.0	0.53	0.189	-8.09	[14]
	10.5	1.1	18.0	-7					[24]
	10.1	5.33[a]	15.1	-5.93[a]					[77]
	9.16		16.14						[73]
Ge	9.75	4.5	16.8	-4.43					[24]
	9.65	4.68[a]	15.5	-4.29[a]					[77]
	9.42		15.13						[73]

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